THE UNIVERSITY OF TEXAS AT AUSTIN Date: 9/13/16

RECOMMENDATION FOR CHANGE IN ACADEMIC RANK/STATUS

Name: Janapa Reddi, Vijay EID: vj239 Present Rank: Assistant Professor

Years of Academic Service ***(Include AY 2016-17 in each count)***:

At UT Austin since: 9/1/2011 (month/day/year) Total Years at UT Austin: 6

In Present Rank since: 9/1/2011 (month/day/year) Total Years in Present Rank: 6

Tenure-track only:
Number of Years in Probationary Status: 5

Additional information: Probationary Extension 2015-16

Primary Department: Electrical and Computer Engineering

College/School: Engineering, Cockrell School of

Joint Department: N/A

College/School: N/A

Other Department(s): N/A

Recommendation actions[1]:

By Budget Council/Executive Committee: Promote

Vote[2] for promotion 31; Against 1; Abstain 2; Absent 0; Ineligible to vote 1

By Department Chair: Promote

By College/School Advisory Committee: Promote

Vote[2] for promotion 7; Against 0; Abstain 0; Absent 0; Ineligible to vote 0

By Dean: Promote

Administrative Action: Promote to Associate Professor

Date Action Effective: September 1, 2017
(To be submitted to the Board of Regents as part of the annual budget.)

By: Maruia M. Tri Date: December 15, 2016
For the President

[1]See "Chart of Recommended Actions" for eligible recommended actions applicable to specific conditions and administrative levels.
[2]Record all votes for and against promotion, abstentions by eligible voting members, and the number of absent eligible voting members. The number of committee members ineligible to vote should also be recorded. Enter zero where it would otherwise be blank.

EVPP/4.15

EXHIBIT
P's 163

Dean's Assessment
Vijay Janapa Reddi
Department of Electrical and Computer Engineering
Cockrell School of Engineering

Dr. Vijay Janapa Reddi received his BS in Computer Engineering from Santa Clara University in 2003, his MS in Electrical and Computer Engineering from the University of Colorado at Boulder in 2006, and his PhD in Computer Science from Harvard University in 2010. Dr. Janapa Reddi worked for one year as a senior design engineer at Advanced Micro Devices, and he joined the Department of Electrical and Computer Engineering (ECE) at the University of Texas at Austin (UT) in September 2011. If successfully promoted to associate professor in September 2017, he will have accumulated five years of probationary service.

This is not an up-or-out case because the 2015-16 academic year did not count toward Dr. Janapa Reddi's probationary service. The department decided to put the case forward one year prior to the mandatory review following a budget council vote in early spring.

Nine external letters were submitted as part of the promotion dossier, of which, five writers were nominated by Dr. Janapa Reddi, and four were selected by the budget council. Seven letter writers are faculty members at universities in the US: Cornell, Princeton, Georgia Tech, Penn State, Stanford, Michigan, and Illinois. One letter writer is a faculty member in Switzerland (Swiss Federal Institute of Technology in Zurich), and one heads the Chrome Cloud Team for Google. Both are former faculty members in the US.

Teaching
Dr. Janapa Reddi's teaching has primarily been in the area of computer engineering with a focus on architecture and embedded systems. During his time in rank, he has taught a total of 223 students in three different courses: EE 319K, *Introduction to Embedded Systems*, a required undergraduate course (taught two times); EE 382V, *Dynamic Compilation*, a graduate course (taught three times); and EE 382V, *Code Generation and Optimization*, a graduate course (taught two times).

Dr. Janapa Reddi's overall average undergraduate instructor rating of 4.35 is higher than the corresponding values for assistant professors in ECE (4.21) and assistant professors in the Cockrell School (4.17). At the graduate level, Dr. Janapa Reddi's overall instructor rating is 4.32, which is slightly less than the average for assistant professors in ECE (4.43) and near the average for assistant professors in the Cockrell School (4.34).

Senior faculty conducted peer evaluations in Dr. Janapa Reddi's courses four times – twice at the undergraduate level and twice at the graduate level. The feedback was positive, but he received multiple suggestions to slow the pace of his presentation and engage the students more during his lectures.

Research
Dr. Janapa Reddi's research encompasses both computer science and computer engineering disciplines. At UT, his research has focused on combined software/hardware engineering solutions for energy-efficient mobile web browsing and development of approaches to monitor and mitigate the effects of voltage noise in various graphical processing unit (GPU) and central processing unit (CPU) architectures. The rapidly increasing use of mobile devices and web-related applications has attracted substantial interest within both academia and industry in Dr. Janapa Reddi's work.

Because the projected use of mobile devices in both the developed and developing world over the coming years is expected to increase substantially, the impact of Dr. Janapa Reddi's work in this area is expected to grow and draw greater attention. Highlights of Dr. Janapa Reddi's research include:

- 20 peer-reviewed conference proceedings (34 total) and two archived refereed journal publications (8 total) in rank. One of his students is the lead author for 12 of the conference proceedings and both journal papers.
- Six of his peer-reviewed conference papers in rank are published in the highly competitive conference proceedings High Performance Computer Architecture (HPCA) or International Symposium on Computer Architecture (ISCA)
- An h-index of 19 (Google Scholar), with 4,220 career citations. One paper describing the Pin tool, which he developed as a graduate student at Colorado, has been cited more than 2,600 times.

While in rank, Dr. Janapa Reddi has secured a total of $2.4 million in external research funding, of which approximately $1.8 million is his share. Dr. Janapa Reddi is the PI on four grants from the National Science Foundation (NSF) totaling nearly $1.4 million, of which his share is approximately $1.0 million. He has also secured over $1.0 million in research funding from industry (Google, Intel, AMD, Samsung, and the Semiconductor Research Corporation), of which his share exceeds $0.8 million.

All nine letters enthusiastically support the promotion of Dr. Janapa Reddi. Many of the referees cite not only his multiple outstanding research achievements, in both computer hardware and software, but also note his unusually high level of creativity and productivity. The referees note that Dr. Janapa Reddi's contributions are not only broadly impacting thinking in computer science and engineering, but are also being incorporated by multiple companies.

David I. August[1] (Princeton) comments, "Dr. Janapa Reddi has already significantly influenced the thinking of and methods used by others in my field." August states "Dr. Janapa Reddi's work has received more academic recognition than the majority of researchers in our field have received in total." August notes the broad nature of Dr. Janapa Reddi's impact in both computer science and engineering and cites his work in tool development (Pin and GPUWattch) and his pioneering work in handling hardware voltage emergencies; he explains "Dr. Janapa Reddi has pioneered the effort ... handling voltage emergencies using a software-assisted, hardware-guaranteed approach." In comparing Dr. Janapa Reddi to peer-level assistant professors across the nation, August writes "... he ranks in the top two in terms of research creativity, productivity, and impact." August concludes his letter by writing, "I am sure that he would be granted tenure at Princeton University ... this tenure case is a "no brainer."

Scott A. Mahlke[2] (Michigan) writes that Dr. Janapa Reddi has had a "... profound impact creating tools that are seamlessly used by students, faculty, and engineers in the computer systems community." Mahlke notes that one "version of [his] technology is being integrated into Samsung's Tizen OS." Mahlke says that Dr. Janapa Reddi is a "trend setter rather than a follower." Mahlke concludes with, "He is clearly over the bar for promotion and tenure, and I strongly urge you to do your best to keep him at Texas."

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[1] Professor of Computer Science
[2] Professor of Electrical Engineering and Computer Science

Chita R. Das[3] (Penn State) remarks "Vijay is internationally known for his research accomplishments in the broad area of computer architecture." Das notes that Janapa Reddi is a "pioneer in ... designing energy-efficient mobile architectures" and that "[his] wimpy core concept has been adopted in several commercial datacenter designs." Das writes that Janapa Reddi's "... research record is simply outstanding" and that he is "one of the best researchers among his peers." Das believes that Janapa Reddi would have "no problem in getting promotion and tenure at Penn State and for that matter in any major school."

David H. Albonesi[4] (Cornell) writes that "Professor Janapa Reddi is a rising star in the computer architecture community" and that he "... has an unusually broad area of impact." Regarding his contributions to the peer-reviewed literature, he notes Janapa Reddi has "... published two papers in ISCA, five in MICRO, and three in HPCA ... more prestigious and competitive than journals ... Overall, this is an outstanding record of achievement." Albonesi notes "The only possible perceived weakness in Professor Janapa Reddi's case might be the lack of an NSF CAREER Award, but I do not consider this a necessary condition for tenure, and the TCCA Young Computer Architect Award more than makes up for it." Albonesi concludes by stating that Janapa Reddi "... would receive tenure here at Cornell."

Advising and Student Mentoring

Dr. Janapa Reddi is currently supervising six PhD students, two of whom have successfully defended and will submit their dissertations to the Graduate School before the deadline for graduation in December. He has also graduated two MS students. Dr. Janapa Reddi has mentored three undergraduate students who worked in his laboratory. He has also hosted fireside chats with Eta Kappa Nu (HKN), the electrical and computer engineering honor society.

University Service

Dr. Janapa Reddi has served on two faculty recruiting committees, and he serves as a bridge linking UT students with industry (e.g., Intel) for internships. Dr. Janapa Reddi has conducted the Hands-on Computer Science (HaCS) program for Austin Independent School District (via UT Outreach).

Professional Service

Dr. Janapa Reddi is serving as the general chair for the 2017 International Symposium on Code Generation and Optimization. He served as the finance chair for the same conference in 2015. While in rank, Dr. Janapa Reddi has participated in nine program committees at various meetings, including the prestigious IEEE High Performance Computer Architecture Symposium and the ACM/IEEE International Symposium on Computer Architecture. In 2014, he served as a program chair for International Symposium on Code Generation and Optimization. Dr. Janapa Reddi has served as a guest editor for two special issues of *IEEE Micro*.

Other Evidence of Merit or Recognition

While in rank, Dr. Janapa Reddi has received multiple awards that recognize his contributions in computer science and engineering. In 2016, he received the Young Computer Architect Award from the Technical Committee on Computer Architecture within the IEEE Computer Society. This award recognizes one individual a year "who has made an outstanding, innovative research contribution or contributions to Computer Architecture." Also in 2016, he gave one of four Gilbreth Lectures during the National Academy of Engineering National Meeting in Irvine, CA. In 2014, Janapa Reddi was invited to participate in the NAE sponsored Indo-American Frontiers of Engineering in Mysore,

[3] Professor of Computer Science and Engineering
[4] Professor of Electrical and Computer Engineering

India. In 2013, Janapa Reddi received an Intel Early Career Award. The award recognizes assistant professors who show great promise as future academic leaders in disruptive computing technologies. He and his students have also received several best paper awards at conferences.

Overall Assessment

Dr. Janapa Reddi has established himself as one of the leading young academics working at the intersection of computer science and computer engineering. His record of teaching is solid. He has established a sustainable research program with funding from the National Science Foundation and various sources in industry. His work in energy efficient web-based mobile applications is widely recognized in both industry and academia. He has presented and published his research at the leading conferences and symposia in his field, at major companies in the industry, and at a number of peer academic institutions. He has received numerous honors and recognition for the work he has completed while at UT. Dr. Janapa Reddi has developed a national standing and is widely recognized as a young emerging leader in computer science and engineering.

Overall, I believe that Dr. Janapa Reddi's performance meets or exceeds expectations for promotion to associate professor with tenure in all categories, and I support this case without reservation.

Sharon L. Wood, Dean
17 October 2016

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
Cockrell School of Engineering

1616 Guadalupe St. • UTA Building, 7th Floor • Austin, Texas 78701
http://www.ece.utexas.edu/

November 4, 2016

Chair's letter in support of the promotion of Prof. Vijay Janapa Reddi to the rank of associate professor with tenure

Prof. Janapa Reddi joined the Department of Electrical and Computer Engineering in August 2011. If promoted to associate professor in September of 2017, he will have served as an assistant professor at the University of Texas at Austin for six years. However, this is technically an early promotion case because Prof. Janapa Reddi had requested an extension to his probationary period due to childbirth.

Vijay is a recognized leader and innovator in the emerging area of co-design of hardware and software to maximize energy efficiency and reliability. The Budget Council recognized his strong accomplishments and potential, and determined that he meets all expectations for promotion at the premier departments of Electrical and Computer Engineering in the nation by a vote of 31 YES, 1 NO and 2 ABSTAIN and 1 INELIGIBLE TO VOTE. One of the two abstains is the departmental representative serving on the Cockrell School of Engineering promotion and tenure committee. He abstained and explained that he did not want to vote twice on the same case. The ineligible is myself. No clear reason was given during the Budget Council discussion or the anonymous comments that we collected for the negative vote and second abstention. Our associate professors voted 18 YES, 0 NO and 0 ABSTAIN in support of promotion.

Third Year Review

The third year review conducted by peers noted that Prof. Janapa Reddi was making satisfactory progress in his research and teaching. In particular, it praised his teaching, invited talks, publication record and funding.

Teaching Load

The normal teaching load for a tenure-track assistant professor is two courses per academic year plus supervision of a senior design team for two semesters. One of the courses must be an undergraduate course. This requirement is waived only under exceptional circumstances if the department has unmet needs at the graduate level. Faculty in the department are routinely given modified instructional duties upon the birth of a child.

Teaching

Prof. Janapa Reddi is an excellent and highly passionate teacher. Since he arrived at UT, he has taught core undergraduate and graduate courses in computer architecture and embedded systems. He has consistently garnered high instruction scores in both his undergraduate and graduate

courses. Indeed, his lowest instructor score is 4.0. Two student comments from the spring of 2016 summarize what many of the students in the last few years have written in their evaluations, "great professor. He clearly explained everything and inspired me to work hard in the course" and "he truly cares for his students." Students however have also complained about his relative lack of organizational skills, particularly towards the end of the semester. Some also complain about the resulting lack of timely feedback. Prof. Janapa Reddi is aware of this issue and is working on improving his organization with the assistance of some of our more experienced instructors. Peers praised his effective teaching and interaction with students. However, some felt that his pace was too fast.

It's worth noting several unique aspects about Prof. Janapa Reddi's teaching. In his undergraduate teaching, he has emphasized hands-on learning. In addition, he has introduced new technology in the classroom, such as Google glass, and leveraged the technology to enhance the delivery of material and personalize learning, even in a large classroom setting. In his graduate classes, he has emphasized practical relevance and impact and succeeded in connecting hardware and software design. Finally, it's worth noting that Prof. Janapa Reddi has also invested substantial time in introducing fifth and sixth graders to computer science by using Arduino boards. His efforts were supported by Intel.

In my mind, Vijay is an excellent model for the faculty at large. He is a great teacher who brings his curiosity and research experience to the classroom, both in what he presents to the students and how he delivers the material by leveraging the latest technology in very innovative and clever ways.

Research

Vijay is already well recognized for his groundbreaking work on hardware and software co-design. While at UT, he has made seminal contributions to mobile web computing that cleverly exploit the interplay between user experience, power consumption and processor capabilities. He has also made highly visible and well-received contributions to resilient energy-efficient Exascale computing. The importance and impact of these contributions cannot be overstressed at a time when improvements in CMOS technology has slowed down, creating a dire need for clever designs that can help designers sustain the mobile and cloud computing revolution. As Prof. Mutlu (ETH, formerly CMU) states, "He has distinguished himself as a leader who has expanded the field of computer architecture in new directions by making outstanding and leading contributions to mobile computer architectures and resilient computer architectures."

Vijay was arguably the first researcher to recognize the importance of hardware and software co-design for energy efficient mobile computing. The importance of this area stems from the explosive growth in the use of web browsing and cloud computing on handheld mobile platforms across the world. In particular, Vijay pioneered the use of Quality of Experience (QoE) to select the most power efficient processor performance that meets the needs of the user in a given context and a given time. He also developed an extensive platform that researchers and engineers can leverage in their work. In particular, he developed GreenWeb, a Web language extension that supports QoE requirements and Wert, a browser runtime that can deliver a desired QoE with minimum power consumption by dynamically adjusting processor cores. He also proposed WebCore, a processor architecture that is optimized for critical mobile computing tasks. Commenting on this work, Dr. Welsh (Google) writes "He is one of the few researchers indeed, the only researcher to my knowledge bringing both architecture and OS ideas to bear on this set of problems… Vijay's work is groundbreaking in terms of exploring this space…I can't overstate how important and difficult this problem is … applying Vijay's ideas to Chrome has the potential for tremendous impact."

His work on resilient energy-efficient Exascale computing is no less impressive. He carefully examined the execution of next-generation machine learning-based datacenter workloads, such as Microsoft's Bing search engine, on low-power mobile processors. His work identified the resulting negative impact on Quality of Service (QoS) robustness and positive impact on power consumption. His work in this area is highly visible and led to a very high profile debate within the computer architecture community. He is also deservedly recognized as the world leading expert on voltage and reliability management on multi-core chips and graphics processors. As energy consumption continues to dominate the design and operation of Exascale computing systems, Vijay identified the interplay between reliability, performance and power consumption, and proposed innovative techniques that deliver high energy efficiency and reliability. His work is based on a clever resilient software-assisted and hardware-guaranteed system design that mitigates emergencies, such as transient power and voltage fluctuations, when they arise, and minimizes the frequency of occurrence of such emergencies. Prof. Kozyrakis (Stanford) agrees with my assessment, and writes that "His paper on datacenter computing with low-power cores sparked one of the most interesting debates in the computer architecture community in the last few years. His proposals on voltage and reliability management on multi-core chips and graphics processors are considered state-of-the-art."

Unlike other academic researchers, Prof. Janapa Reddi has also developed and made public a set of tools, such a Pin and more recently Simulation Analysis Engine, that are very popular with researchers and practitioners, as noted by several reference letter writers. These tools have multiplied the impact and influence of his work.

Prof. Janapa Reddi is very well funded by highly competitive peer-reviewed grants from NSF. He also has significant industry funding from Google, Intel, AMD and SRC. While he hasn't received an NSF CAREER award, he did receive an Intel Early Career award. As Prof. Albonesi (Cornell) notes, "The Intel Early Career and Google Faculty Research awards are both highly competitive and indicate the strong industry interest in Professor Janapa Reddi's research." He is held in high esteem by his colleagues, as evidenced by the number of invited high visibility talks that he has given and the TCCA Young Computer Architect Award that he recently received.

Our department has adopted the practice of comparing each colleague with his or her most prominent peers at the first-tier departments in Electrical and Computer Engineering, such as MIT, Stanford, the University of California Berkeley, the University of Illinois Urbana-Champaign (UIUC), Georgia Tech, Caltech and Princeton. My colleagues and I selected Associate Profs. Ceze (Washington), Kumar (UIUC), Wenisch (Michigan) and Narayanasamy (Michigan). These associate professors were promoted in 2012, 2013, 2013 and 2014 respectively. I note that Washington has one of the strongest computer science departments in the Nation. Vijay compares very favorably to Kumar and Narayanasamy in terms of publications in top selective conferences and journals at time of promotion, and h-index. Ceze and Wenisch had more publications in selective conferences at time of promotion than Vijay and have a higher h-index. However, they had lower numbers of journal publications than Vijay. Ceze also received the TCCA Young Computer Architect Award. I would argue that Vijay has had as much or more influence on the field than all four associate professors in this peer group, as also stated in several letters. Indeed, Prof. Torrellas (UIUC) nicely summarizes what was stated in several letters when he writes, "Prof. Reddi's work is influential. It is being followed by other researchers (for example, I do), and by industry." The letter writers provide additional comparisons and invariably conclude that Vijay is as good as, or better than, the best computer architects in academia today.

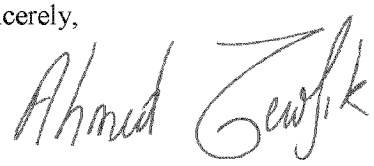
Service

Vijay has provided excellent service to both UT and the profession. Details can be found in his resume and the budget council statement.

Summary

Vijay is an excellent teacher and a recognized leader in hardware software co-design and energy efficient design. He has served UT and his profession well. I strongly endorse his promotion to associate professor with tenure.

Sincerely,



Prof. Ahmed H. Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

DRAFT of Third-Year Review
Dr. Vijay Janapa Reddi
Assistant Professor of Electrical and Computer Engineering

January 15, 2014

Prepared by Professors Perry, and Baccelli

This third-year review for Prof. Vijay Janapa Reddi covers his research, teaching, and service to The University of Texas at Austin during the three academic years from 2011-2012 to 2013-2014, inclusive. Prof. Janapa Reddi joined UT Austin as an Assistant Professor of Electrical and Computer Engineering (ECE) in Fall 2011.

Teaching

Prof. Janapa Reddi has taught the following courses at UT Austin while in rank:

Semester	*Course*	*# Surveys / Enrollment*	*Overall Instr. Rating*	*Overall Course Rating*
Spring 2012	EE382V Dynamic Compilation	19/21	4.0	3.4
Fall 2012	EE382V Code Gen & Opt	13/16	4.5	4.2
Spring 2013	EE382V Dynamic Compilation	8/8	4.4	4.1
Fall 2013	EE382V Code Gen & Opt	26/29	4.4	4

Average CIS Score for U/G =4.01, for Grad = 4.19
Department Average CIS Score for U/G = 4.07, for Grad = 4.22

Prof. Janapa Reddi developed and introduced two new graduate courses in his 3 years: EE382V Dynamic Compilation and Code Generation and Optimization. He has taught the dynamic compilation course twice and the code generation and optimization course once. An undergraduate version of the code generation and optimization course was offered in the fall of 2013.

Research

Two important measures of an ECE professor's research output are (1) quality and impact of peer-reviewed publications, and (2) quality and impact of PhD students graduated.

At UT Austin, since the fall of 2011, Prof. Janapa Reddi has published or had accepted for publication 9 peer-reviewed journal and conference papers, two workshop papers, one patent, as well as a number tutorials. He has also been invited for talks at prestigious venues such as the National Academy of Engineering. Extremely rare for someone at this stage in his career is the publication of a monograph. He received a Top Picks in Computer Architecture award from IEEE Micro, 2011. He also received the Intel Early Career Award in 2013 for his distinguished approach to Computer Architecture research involving hardware and software co-design. His overall career publication and citation record are very impressive. He has received 2355 citations (H Index of 15). His most notable research work has 1759 citations.

Once an ECE faculty member has built his/her research group, he/she is expected to graduate one PhD student each year on average. Prof. Janapa Reddi has graduated two MS students – Aditya Srikanth (Chair) and Ankita (Garg) Goel (Co-Chair). He currently has six PhD students: Yuhao Zhu, Matthew Halpern, Jingwen Leng, Yazhou Zu, Wooseok Lee and Ahmad El Youseff. In addition, he is on the committee of 5 PhD students. He appears to be on track to meet the standard requirement of a graduated PhD student.

Research funding enables support of graduate students to conduct research. ECE faculty members average about $200,000 per year of his/her share of external research funding. Prof. Janapa Reddi has already brought in approximately $1,085,000 in external research funding. In particular, he has won two highly competitive grants from the National Science Foundation. In addition, he has been awarded an Intel Early Career Award, and two Google Faculty Research Awards. He is doing extremely well in raising external research funding after three years as an Assistant Professor.

Service

Prof. Janapa Reddi has an extraordinary professional service record that far surpasses the norm at this point in an academic research career: the Program Chair and on the Steering Committee for the IEEE International Symposium on Code Generation and Optimization (a premier venue for Compiler research), the organizer of 7 workshops, a guest editor of a special issue, publications, tutorial, and local arrangements chair positions, and is a member of 10 program committees for top general and specialty conferences and workshops. He has also served as an external review committee in formal capacity for several journals and conferences. We expect this level of involvement to continue and increase appropriately as his career advances

Summary

Prof. Janapa Reddi's teaching, research and service records place him on track for tenure and promotion. His research record including publications, invited talks, and external grants are truly exemplary. His professional service participation is extremely strong and steadily increasing.

THE UNIVERSITY OF TEXAS AT AUSTIN

Cockrell School of Engineering

FULL NAME: Vijay Janapa Reddi

TITLE: Assistant Professor

DEPARTMENT: Electrical and Computer Engineering

RESEARCH AREAS: Computer Architecture; Compilers; Runtime Systems.

EXPERTISE DOMAINS: Mobile Computing; High-Performance Systems; Web Technologies.

EDUCATION:

Harvard University	Computer Science	Ph.D.	2010
University of Colorado—Boulder	Electrical and Computer Engineering	M.S.	2006
Santa Clara University	Computer Engineering	B.S.	2003

CURRENT AND PREVIOUS ACADEMIC POSITIONS:

University of Texas at Austin	Assistant Professor	August 2011 – Present

OTHER PROFESSIONAL EXPERIENCE:

Intel	Consultant	June 2015 – Present
Advanced Micro Devices (AMD)	Consultant	February 2015 – Present
Intel	Consultant	June 2014 – August 2014
Advanced Micro Devices (AMD)	Senior Design Engineer	July 2010 – July 2011
Microsoft Research	Research Intern	March 2009 – June 2009
VMware	Research Intern	January 2007 – March 2009
Intel	Research Intern	April 2003 – December 2006

HONORS AND AWARDS:

- IEEE TCCA Young Computer Architect Award, *IEEE Computer Society*, 2016.
- Top Picks Honorable Mention in Computer Architecture, *IEEE Micro*, 2016.
- Gilbreth Lectureship Award, *National Academy of Engineering (NAE)*, 2016.
- Most Influential PLDI Paper Award, *ACM SIGPLAN*, 2015.
- Indo-American Frontiers of Engineering, *National Academy of Engineering (NAE)*, 2014.
- Intel Early Career Honor Award, *Intel*, 2013.
- Google Faculty Research Award, *Google*, 2012, 2013, 2015.
- Top Picks in Computer Architecture, *IEEE Micro*, 2011.
- Top Picks in Computer Architecture, *IEEE Micro*, 2010.
- Best Paper Award, *Intl. Symp. on High Performance Computer Architecture (HPCA)*, 2009.
- John A. and Elizabeth S. Armstrong Fellowship, *Harvard University*, 2008.
- Best Student Presentation, *Intl. Symp. on Code Generation and Optimization (CGO)*, 2007.
- Top Picks in Computer Architecture, *IEEE Micro*, 2006.
- Best Paper Award, *International Symposium on Microarchitecture (MICRO)*, 2005.
- Faculty Recognition for Technical Excellence, *Santa Clara University*, 2003.
- Outstanding Undergraduate (Honorable Mention), *Computing Research Association (CRA)*, 2003.

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES:

Member: Institute of Electrical and Electronics Engineers (IEEE)
Member: Association for Computing Machinery (ACM)

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental-	Member, Faculty Recruiting Committee	2015
	Member, Technology in Teaching	2014
	Member, Faculty Recruiting Committee	2013
	Graduate Student Admissions Committee	2011- Present

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES:

- General Chair, Intl. Symp. on Code Generation and Optimization (CGO 2017)
- Finance Chair, Intl. Symp. on Code Generation and Optimization (CGO 2015)
- Program Committee,
  - Intl. Symp. on Computer Architecture (ISCA 2014)
  - High Performance Computer Architecture (HPCA 2012, 2014, 2015)
  - Microarchitecture (MICRO 2013,2014)
  - Principles and Practice of Parallel Computing (PPoPP 2013, 2015)
  - Code Generation and Optimization (CGO 2013, 2014)
  - Parallel Architectures and Compilation Techniques (PACT 2013)
  - Workload Characterization (IISWC 2012, 2013, 2016)
  - Parallel & Distributed Processing (IPDPS 2012)
  - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2012)
- Program Chair, Intl. Symp. on Code Generation and Optimization (CGO 2014)
- Guest Editor,
  - IEEE Micro Special Issue on Reliability-Aware Microarchitecture Design (2013),
  - IEEE Micro Special Issue on Internet of Things (2016)

- Local Arrangements Chair,
  - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2013)
  - Workshop on Silicon Errors in Logic - System Effects (SELSE 2015, 2016)
- Publications Chair, Intl. Symp. on Workload Characterization (IISWC 2013)
- Organizer
  - Tutorial on Tools for Mobile Computer Architecture (MobiTools 2016)
  - Tutorial on Simulation and Analysis Engine (ISCA 2016, ASPLOS 2016, HPCA 2016, ICS 2016, IISWC 2015, ISPASS 2015)
  - Workshop on Resilient Architectures (WRA 2013–2010)
- Steering Committee, Intl. Symp. on Code Generation and Optimization (CGO)

COMMUNITY ACTIVITIES:

- Hands-on Computer Science (HaCS) for Austin Independent School District (via UT Outreach), https://outreach.uteach.utexas.edu/csp

PUBLICATIONS:

Google Scholar link, https://scholar.google.com/citations?user=gy4UVGcAAAAJ&hl=en&oi=ao

Refereed Conference Proceedings (34 Papers)

C1. T. Moseley, A. Shye, **V. Janapa Reddi**, M. Iyer, D. Fay, J. Kihm, A. Settle, D. Grunwald, D. Connors. "Dynamic Run-time Architecture Techniques for Enabling Continuous Optimization," in *ACM International Conference on Computing Frontiers (CF)*, pp.211-220, May 2005. http://dx.doi.org/10.1145/1062261.1062296

C2. C. Luk, R. Cohn, R. Muth, H. Patil, A. Klauser, G. Lowney, S. Wallace, **V. Janapa Reddi**, K. Hazelwood. "Pin: Building Customized Program Analysis Tools with Dynamic Instrumentation," in *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, vol 40(6), pp.190-200, June, 2005. http://dx.doi.org/10.1145/1064978.1065034

C3. S. Figueira, **V. Janapa Reddi**. "Topology-Based Hypercube Structures for Global Communication in Heterogeneous Networks," in *Euro-Par*, pp.994-1004, September 2005. http://dx.doi.org/10.1007/11549468_109

C4. A. Shye, M. Iyer, **V. Janapa Reddi**, D. Connors. "Code Coverage Testing Using Hardware Performance Monitoring Support," in *IEEE International Symposium on Automated and Analysis-Driven Debugging (AADEBUG)*, pp.159-163, September 2005. http://dx.doi.org/10.1145/1085130.1085151

C5. Q. Wu, **V. Janapa Reddi**, Y. Wu, J. Lee, D. Connors, M. Martonosi, D. Clark. "A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp.12-282, November 2005. http://dx.doi.org/10.1109/micro.2005.7

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C12. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Web Search Using Mobile Cores: Quantifying and Mitigating the Price of Efficiency," in *ACM/IEEE International Symposium on Computer Architecture (ISCA)*, vol 38(3), pp.314-325, June 2010. http://dx.doi.org/10.1145/1816038.1816002

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C21. C. Zhou, X. Wang, W. Xu, Y. Zhu, **V. Janapa Reddi,** C. Kim. "Estimation of Instantaneous Frequency Fluctuation in a Fast DVFS Environment Using an Empirical BTI Stress-Relaxation Model," *in IEEE International Symposium on International Reliability Physics Symposium (IRPS)*, pp.2D.2.1-2D.2.6, June 2014. http://dx.doi.org/10.1109/irps.2014.6860593

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C25. M. Halpern, Y. Zhu, R. Peri, **V. Janapa Reddi**. "Mosaic: Cross-Platform User-Interaction Record and Replay for the Fragmented Android Ecosystem," in *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp.215-224, March 2015. http://dx.doi.org/10.1109/ispass.2015.7095807

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C27. Y. Zu, C. R. Lefurgy, J. Leng, M. Halpern, M. S. Floyd, **V. Janapa Reddi**. "Adaptive Guardband Scheduling to Improve System-level Efficiency of the POWER7+," in *IEEE International Symposium on Microarchitecture (MICRO)*, pp.308-321, December 2015. http://dx.doi.org/10.1145/2830772.2830824

C28. Y. Zhu, D. Richins, M. Halpern, **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Server-side Web Applications," in IEEE *International Symposium on Microarchitecture (MICRO)*, pp.762-774, December 2015. http://dx.doi.org/10.1145/2830772.2830792

C29. M. Halpern, Y. Zhu, **V. Janapa Reddi**. "Mobile CPU's Rise to Power: Quantifying the Impact of Generational Mobile CPU Design Trends on Performance, Energy, and User Satisfaction," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.64-76, March 2016. http://dx.doi.org/10.1109/hpca.2016.7446054

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C31. Y. Liu, Z. Yu, L. Eeckhout, **V. Janapa Reddi**, Y. Luo, X. Wang, Z. Wang, C. Xu. "Barrier-Aware Warp Scheduling for Throughput Processors," in *ACM International Conference on Supercomputing (ICS)*, June 2016. http://dx.doi.org/10.1145/2925426.2926267

C32. N. Chachmon, D. Richins, R. Cohn, M. Christensson, W. Cui, **V. Janapa Reddi**. "Simulation and Analysis Engine for Scale-out Workloads," in *ACM International Conference on Supercomputing (ICS)*, June 2016. http://dx.doi.org/10.1145/2925426.2926293

C33. Y. Zu, W. Huang, I. Paul, **V. Janapa Reddi**. "Ti states: Processor Power Management in the Temperature Inversion Region," in IEEE *International Symposium on Microarchitecture (MICRO)*, October 2016. Accepted.

C34. M. Kazdagli, **V. Janapa Reddi**, M. Tiwari. "Quantifying and Improving the Efficiency of Hardware-based Mobile Malware Detectors," in IEEE *International Symposium on Microarchitecture (MICRO)*, October 2016. Accepted.

Refereed Journal Proceedings (8 Papers)

J1. Q. Wu, M. Martonosi, D. Clark, **V. Janapa Reddi**, D. Connors, Y. Wu, J. Lee, D. Brooks. "Dynamic-Compiler-Driven Control for Microprocessor Energy and Performance," in IEEE *Micro's Top Picks in Computer Architecture*, vol 26(1), pp.119-129, January 2006. http://dx.doi.org/10.1109/mm.2006.9

J2. A. Shye, J. Bloomstedt, T. Mosely, **V. Janapa Reddi**, D. Connors. "PLR: A Software Approach to Transient Fault Tolerance for Multicore Architectures," in IEEE *Transactions on Dependable and Secure Computing (TDSC)*, vol 6(2), pp.135-148, November 2008. http://dx.doi.org/10.1109/tdsc.2008.62

J3. **V. Janapa Reddi**, M. Gupta, M. Smith, G. Wei, D. Brooks, K. Hazelwood. "Eliminating Voltage Emergencies via Software-Guided Code Transformations," in *ACM Transactions on Architecture and*

Code Optimization (TACO), vol 7(2), pp.1-28, September 2010. http://dx.doi.org/10.1145/1839667.1839674

J4. **V. Janapa Reddi**, M. Gupta, G. Holloway, M. Smith. "Predicting Voltage Droops Using Recurring Program and Microarchitectural Event Activity," in IEEE *Micro's Top Picks in Computer Architecture*, vol 30(1), p.110, January 2010. http://dx.doi.org/10.1109/mm.2010.25

J5. **V. Janapa Reddi**, S. Kanev, W. Kim, S. Campanoni, M. Smith, G. Wei, D. Brooks. "Voltage Noise in Production Processors," in IEEE *Micro's Top Picks in Computer Architecture*, vol 31(1), pp.20-28, February 2011. http://dx.doi.org/10.1109/mm.2010.104

J6. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Mobile Processors for Energy-Efficient Web Search," in *ACM Transactions on Computer Systems (TOCS)*, vol 29(3), art.9, August 2011. http://dx.doi.org/10.1145/2003690.2003693

J7. Y. Zhu, A. Srikanth, J. Leng, **V. Janapa Reddi**. "Exploiting Webpage Characteristics for Energy-Efficient Mobile Web Browsing," in IEEE *Computer Architecture Letters (CAL)*, pp.33-36, October 2012. http://dx.doi.org/10.1109/l-ca.2012.33

J8. Y. Zhu, M. Halpern, **V. Janapa Reddi**. "The Role of the CPU in Energy-Efficient Mobile Web Browsing," in IEEE *MICRO — Special issue on Mobile Systems*, vol. 35(1), pp. 26-33, January 2015. http://dx.doi.org/10.1109/mm.2015.8

Books and Manuscripts (1 Book)

B1. **V. Janapa Reddi** and M. Gupta. *Resilient Architecture Design for Voltage Variation*, Synthesis Lectures on Computer Architecture, Morgan & Claypool Publishers, vol 8(2), pp.1-138, June 2013. http://dx.doi.org/10.2200/s00486ed1v01y201303cac022

Workshops (10 Papers)

W1. **V. Janapa Reddi**, A. Settle, D. Connors, R. Cohn. "PIN: A Binary Instrumentation Tool in Computer Architecture Research and Education," in *International Workshop on Computer Architecture Education (WCAE)*. June 2004. http://dx.doi.org/10.1145/1275571.1275600

W2. A. Shye, M. Iyer, T. Mosely, D. Hodgdon, D. Fay, **V. Janapa Reddi**, D. Connors. "Analysis of Path Profiling Information Generated with Performance Monitoring Hardware," in *ACM SIGARCH Workshop on Interaction between Compilers and Computer Architecture (INTERACT)*, pp. 33-43, February 2005. http://dx.doi.org/10.1109/interact.2005.3

W3. **V. Janapa Reddi**, D. Connors, R. Cohn. "Persistence in Dynamic Code Transformation Systems," in *ACM SIGARCH Workshop on Binary Instrumentation and Applications (WBIA)*, vol 33(5), pp. 69-74, December 2005. http://dx.doi.org/10.1145/1127577.1127591

W4. A. Shye, **V. Janapa Reddi**, T. Moseley, D. Connors. "Transient Fault Tolerance via Dynamic Process Redundancy," in *ACM SIGARCH Workshop on Binary Instrumentation and Applications (WBIA)*. October 2006.

W5. **V. Janapa Reddi**, M. Gupta, K. Rangan, S. Campanoni, G. Holloway, M. D. Smith, G. Wei, D. Brooks. "Voltage Noise: Why It's Bad, and What to Do About It," in *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*. March 2009.

W6. S. Kanev, T. M. Jones, G. Wei, D. Brooks, **V. Janapa Reddi**. "Measuring Code Optimization Impact on Voltage Noise," in *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*. March 2013.

W7. L. Guckert, M. O' Connor, S. Kumar Ravindranath, Z. Zhao, **V. Janapa Reddi**. "A Case for Persistent Caching of Compiled JavaScript Code in Mobile Web Browsers," in *Workshop on Architectural and Microarchitectural Support for Binary Translation*. March 2013.

W8. J. Leng, Y. Zu, **V. Janapa Reddi**. "Energy Efficiency Benefits of Reducing the Voltage Guardband on the Kepler GPU Architecture," in *IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE)*. March 2014.

W9. S. Chai, D. Zhang, J. Leng, **V. Janapa Reddi**. "Lightweight Detection and Recovery Mechanisms to Extend Algorithm Resiliency in Noisy Computation," in *Workshop on Nearthreshold Computing* (co-located with ISCA), June 2014.

W10. M. Kazdagli, L. Huang, **V. Janapa Reddi**, M. Tiwari. "Morpheus: Benchmarking Computational Diversity in Mobile Malware," in Workshop on Hardware and Architectural Support for Security and Privacy. June 2014. http://dx.doi.org/10.1145/2611765.2611767

Technical Reports (1 Paper)

R1. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Web Search Using Small Cores: Quantifying the Price of Efficiency," in Microsoft Research Tech. Report, June 2010.

Theses (3 Papers)

Th1. **V. Janapa Reddi**. "Heterogeneous Networks of Workstations Across Wide Area Networks," B.S. Thesis, Department of Electrical and Computer Engineering, Santa Clara University. June 2003.

Th2. **V. Janapa Reddi**. "Deploying Dynamic Code Transformation in Modern Computing Environments," M.S. Thesis, Department of Electrical and Computer Engineering, University of Colorado. November 2005.

Th3. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability: Enabling Aggressive Timing Speculation Using Run-Time Feedback from Hardware and Software," Ph.D. Thesis, School of Engineering and Applied Sciences, Harvard University. March 2010.

ORAL PRESENTATIONS:

Invited Talks and Seminars

O1. **V. Janapa Reddi**. "Persistent Code Caching," Intel, Santa Clara–CA, March 2007.

O2. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Intel, Santa Clara–CA, March 2010.

O3. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," AMD, Austin–TX, March 2010.

O4. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Microsoft Research, Redmond–WA, June 2010.

O5. **V. Janapa Reddi**. "Web Search Using Small Cores," Amazon, Seattle–WA, June 2010.

O6. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Intel, Portland–OR, July 2010.

O7. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," IBM T. J. Watson Labs, Yorktown–NY, July 2010.

O8. **V. Janapa Reddi**. "Web Search Using Small Cores," SeaMicro, Santa Clara–CA, July 2010.

O9. **V. Janapa Reddi**. "Web Search Using Small Cores," Google, Palo Alto–CA, July 2010.

O10. **V. Janapa Reddi**. "Web Search Using Small Cores," HP Labs, Palo Alto–CA, July 2010.

O11. **V. Janapa Reddi**. "Web Search Using Small Cores," Facebook, Palo Alto–CA, July 2010.

O12. **V. Janapa Reddi**. "Web Search Using Small Cores," IBM T. J. Watson Labs, Hawthorne–NY, July 2010.

O13. **V. Janapa Reddi**. "Web Search Using Small Cores," Intel, Hudson–MA, July 2010.

O14. **V. Janapa Reddi**. "Web Search Using Small Cores," AMD, Boxborough–MA, October 2010.

O15. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," Intel, Austin–TX, August 2012.

O16. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," *AMD*, Austin–TX, August 2012.

O17. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," Qualcomm, Santa Clara–MA, February 2013.

O18. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," Intel, Austin–TX, February 2014.

O19. **V. Janapa Reddi**. "Robust and Resilient Systems from the Bottom-Up: Circuits, Architecture and Software Integration," ISSCC Forum, San Francisco–CA, February 2014.
O20. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," Samsung, Austin–TX, March 2014.
O21. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," *ARM*, Austin–TX, March 2014.
O22. **V. Janapa Reddi**. "Mobile Processor Architectures: Design Implications and Challenges for Energy Efficiency," Indo-American Frontiers of Engineering (IAFOE), Mysore–India, May 2014.
O23. **V. Janapa Reddi**. "Hardware and Software Co-Design for Robust and Resilient Execution," International Conference on Integrated Circuit Design and Technology (ICICDT), Austin–TX, May 2014.
O24. **V. Janapa Reddi**. "Architecting for the Mobile Web: Where We've Been, Where We're Heading, and What We Need to Address," Parallelism in Mobile Platforms (PRISM) held in conjunction with International Symposium on Computer Architecture, June 2014.
O25. **V. Janapa Reddi**. "Simulators are Perfect, Authors are Oracles, Users are Innocent," Workshop on Duplicating, Deconstructing and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture, June 2014.
O26. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Univ. of Michigan, November 2014.
O27. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Intel, Santa Clara–CA, February 2015.
O28. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Facebook, Menlo Park–CA, March 2015.
O29. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Microsoft, Seattle–WA, April 2015.
O30. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Qualcomm, Raleigh–NC, April 2015.
O31. **V. Janapa Reddi**. "Voltage Noise in Multicore Processors," Intel, Portland–OR, May 2015.
O32. **V. Janapa Reddi**, "GPU Voltage Guardband Management to Achieve Exascale Energy-Efficiency," Intel, Portland–OR, May 2015.
O33. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Duke University, Raleigh–NC, June 2015.
O34. **V. Janapa Reddi**. "GPU Voltage Guardband Management to Achieve Exascale Energy-Efficiency," *AMD*, Austin–TX, June 2015.
O35. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Taiwan Application Processor Union – Mobile SoC Summer Course, Taiwan, September 2015.
O36. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Mediatek, Taiwan, September 2015.
O37. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," National Taiwan University, Taiwan, September 2015.
O38. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Academia Sinica, Taiwan, September 2015.
O39. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Georgia Tech University, October 2015.
O40. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Google Faculty Summit, October 2015.
O41. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Texas A&M University, November 2015.

O42. **V. Janapa Reddi**. "Programming the Web of Things," Workshop on Internet of Things (IoT) held in conjunction with International Symposium on Microarchitecture, Hawaii, December 2015.
O43. **V. Janapa Reddi**. "End of the Road for My CAREER," Workshop on Negative Outcomes, Post-mortems, and Experiences (NOPE) held in conjunction with International Symposium on Microarchitecture, Hawaii, December 2015.
O44. **V. Janapa Reddi**. "From Moore's Law to Moore's Crawl: Architecting the Next-Generation of Mobile Computing Devices," University of Washington, Seattle–WA, February 2016.
O45. **V. Janapa Reddi**. "From Moore's Law to Moore's Crawl: Architecting the Next-Generation of Mobile Computing Devices," National Academy of Engineering (NAE) Annual Event, Irvine–CA, February 2016.
O46. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Rice University – TexasWISE Keynote, Houston, May 2016.
O47. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," Intel, Santa Clara–CA, May 2016.
O48. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," AMD, Austin–TX, May 2016.
O49. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," Northwestern, Chicago–IL, May 2016.
O50. **V. Janapa Reddi**. "Watt-WiseWeb://Architecting for Responsiveness and Energy-Efficiency," The University of Chicago, Chicago–IL, May 2016.

Other Major Presentations

T1. R. Cohn and **V. Janapa Reddi**. "Software Instrumentation and Hardware Profiling for Intel Itanium Linux," International Symposium on Code Generation and Optimization (CGO), 2004.
T2. C. Luk, D. Connors, W. Hsu, T. Moseley, **V. Janapa Reddi**. "Software Instrumentation as a Tool for Architecture and Compiler Research," International Symposium on Architectural Support for Programming Languages and Operating (ASPLOS), 2004.
T3. K. Hazelwood and **V. Janapa Reddi**. "Using Pin for Compiler and Computer Architecture Research and Education," International Symposium on Programming Language Design and Implementation (PLDI), 2007.
T4. K. Hazelwood, **V. Janapa Reddi**, D. Kaeli, D. Connors. "Hands-on Pin! for Architecture, OS and Program Analysis Research," International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2007.
T5. S. Campanoni and **V. Janapa Reddi**. "ILDJIT Compiler Framework for Architecture Research," International Symposium on Microarchitecture (MICRO), 2010.
T6. **V. Janapa Reddi.** "Hardware and Software Co-design for Robust and Resilient Execution," International Conference on IC Design and Technology (ICICDT), 2012.
T7. N. Chachmon, M. Christensson, R. Cohn, **V. Janapa Reddi.** "SIMICS 2015: System-level Program Analysis and Architectural Evaluation with Simics," International Symposium on Performance Analysis of Systems and Software (ISPASS), 2015.
T8. N. Chachmon, M. Christensson, R. Cohn, **V. Janapa Reddi.** "SIMICS 2015: System-level Program Analysis and Architectural Evaluation with Simics," International Symposium on Workload Characterization (IISWC), 2015.
T9. N. Chachmon, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on High Performance Computer Architecture (HPCA,), 2016.
T10. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2016.

T11. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Conference on Supercomputing (ICS), 2016.
T12. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on Computer Architecture (ISCA), 2016.
T13. Y. Zhu, M. Halpern, **V. Janapa Reddi.** "MobiTools: Tutorial on Infrastructure and Tools for Mobile Computer Architecture Research with an Emphasis on Real System Measurement," International Symposium on Computer Architecture (ISCA), 2016.
T14. D. Richins, B. Gowda, N. Chachmon, M. Christensson, **V. Janapa Reddi.** "BigBench+SAE: Instrumenting an Industry-strength BigData Benchmark for BigData Analytics," International Symposium on Microarchitecture (MICRO), 2016.

PATENTS:

P1. R. Cohn, T. Moseley, and **V. Janapa Reddi**. "System and method to instrument references to shared memory." U.S. Patent Application 11/143,130, filed June 1, 2005.
P2. N. Kim, J. O'Connor, M. Schulte, and **V. Janapa Reddi**. "Method and apparatus for power reduction during lane divergence." U.S. Patent Application 13/605,460, filed September 6, 2012.
P3. **V. Janapa Reddi,** M. Gupta, G. Holloway, G. Wei, M. D. Smith, and D. Brooks. "Adaptive event-guided system and method for avoiding voltage emergencies." U.S. Patent 8,949,666, issued February 3, 2015.

GRANTS, CONTRACTS and GIFTS:

Grants and Contracts

PI/Co-PI	Title	Agency	Grant Period	Total/ My Share
PI Janapa Reddi (self)	High-Performance, Energy-Efficient Mobile Web Computing	National Science Foundation	06/01/2016 - 05/31/2019	$400,000/ $400,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Second Phase of Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	04/10/2015 - 01/10/2016	$100,000/ $43,500
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-Driven Resiliency for Near-Threshold Systems: under SRC MAG (201300745-001;2013-HJ-2408 MAG)	Semiconductor Research Corporation	04/01/2013 - 03/31/2017	$128,000/ $64,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	12/15/2013 - 01/15/2015	$100,000/ $43,500

PI Janapa Reddi/ Co-PI Sek Chai (SRI)	Resilient Computing Systems Using Deep Learning Techniques	National Science Foundation	08/01/2015 - 07/31/2018	$499,959/ $265,000
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-driven resiliency for Near Threshold Systems	National Science Foundation	04/01/2013 - 03/31/2016	$192,000/ $96,000
PI Janapa Reddi/ Co-PI Lizy John (UT Austin)	Cross-Layer Solutions for Sustainable and Reliable Computing Solutions	National Science Foundation	08/01/2012 - 07/31/2015	$300,000/ $214,670

Industry Gifts

PI/Co-PI	Title	Agency	Grant Period	Grant Total
PI Janapa Reddi (self)	Mobile computing	Google	2012, 2013, 2015	$139,000
PI Janapa Reddi (self)	Reliability and Mobile Computing	Intel	2012, 2013, 2015, 2016	$395,000
PI Janapa Reddi (self)	Power modeling	AMD	2012, 2013, 2014, 2015	$150,000
Total Funding:				**$2,403,959**
My Total Funding:				**$1,810,670**

PH.D. STUDENTS:

A. Students defended
   a. Jingwen Leng (passed, expected graduation December 2016)

B. Students in candidacy, passed Ph.D. qualifying exam
   a. Yuhao Zhu

C. Post M.S. students, preparing to take Ph.D. qualifying exam
   a. Matthew Halpern
   b. Daniel Richins

D. Passed Ph.D. pre-qualifying exam
   a. Wenzhi Cui
   b. Yazhou Zu

M.S. STUDENTS:

A. Students graduated:
   a. Srikanth, Aditya (May 2013)
   b. Garg, Ankita (co-supervised, May 2013)

BRIEF VITA:

Vijay Janapa Reddi is an Assistant Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. His research interests span the definition of computer architecture, including software design and optimization, to enhance mobile quality-of-experience and improve the energy-efficiency of high-performance computing systems. Dr. Janapa Reddi is a recipient of the National Academy of Engineering Gilbreth Lectureship honor (2016), IEEE Computer Society TCCA Young Computer Architect Award (2016), Intel Early Career Award (2013) and multiple Google Faculty Research Awards (2012, 2013, 2015). He is also the recipient of the Best Paper at the 2005 International Symposium on Microarchitecture, Best Paper at the 2009 International Symposium on High-Performance Computer Architecture, and IEEE's Top Picks in Computer Architecture awards (2006, 2010, 2011). Beyond his scientific research contributions, Dr. Janapa Reddi is passionate about starting STEM education at an early age. He is responsible for the Austin Independent School District's "hands-on" computer science (HaCS) program, which teaches 5th and 6th-grade students programming and the principles that govern a modern computing system using Arduino devices. He received a BS in computer engineering from Santa Clara University, an MS in electrical and computer engineering from the University of Colorado at Boulder, and a Ph.D. in computer science from Harvard University.

Master Promotion Summary for "In Rank"
Vijay Janapa Reddi

Metric	Value
Peer-reviewed journal publications (in rank ***and total)***	3 / 8
Peer-reviewed conference proceedings (in rank ***and total)***	20 / 34
Number of ***journal*** papers ***in rank*** with UT students ***as co-authors***	2
Total citations of all publications (career) ***from ISI Web of Knowledge***	333
h-index (career) ***from ISI Web of Knowledge****	7
Total citations of all publications (career) ***from Google Scholar or Publish or Perish***	4220**
h-index (career) ***from Google Scholar or Publish or Perish*** *	19
Total external research funding raised	$2,403,959
Total external research funding raised (candidate's share)	$1,810,670
Total number of external grants/contracts ***awarded***	7
Number of external grants/contracts ***awarded*** as PI	5
PhD students completed†	0
MS students completed†	1.5
PhD students in pipeline (as of 09/2016) †	6
MS students in pipeline (as of 09/2016) †	0
Number of courses taught	7
Total # of students taught in organized courses	229
Average instructor evaluation for UG courses	4.4
Average instructor evaluation for Grad courses	4.3
Average course evaluation for UG courses	4.1
Average course evaluation for Grad courses	4.0
Teaching awards	N/A
Student organizations advised	0
Undergraduate ***researchers*** supervised	3
Service on journal editorial boards	2
Number of symposia organized	2

Provide a printout/screen shot of the first page of the report from both ISI Web of Knowledge and Google Scholar

† Count a student as 1.0 if sole supervisor and 0.5 if co-supervised.

**Citation counts were pulled on Jun. 16, 2016.

Complete reverse chronological list of publications and scholarly/creative works

Vijay Janapa Reddi

Title of Dissertation:
"Software-Assisted Hardware Reliability: Using Runtime Feedback from Hardware and Software to Enable Aggressive Timing Speculation"

Dissertation Advisor:
David Brooks, Harvard University.

Section 1. Works published (or in an equivalent status), in press, accepted, or under contract while in current rank at UT Austin.

A. Refereed Conference Proceedings

- Y. Zu, W. Huang, I. Paul, **V. Janapa Reddi**. "Ti states: Processor Power Management in the Temperature Inversion Region," in IEEE International Symposium on Microarchitecture (MICRO), October 2016 (Accepted).
  - A. Co-authors:
    - i. Y. Zu — The University of Texas at Austin, my student
    - ii. W. Huang — Advanced Micro Devices (AMD)
    - iii. I. Paul — Advanced Micro Devices (AMD)
    - iv. V. Janapa Reddi — The University of Texas at Austin
  - B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work. The AMD co-authors provided access to physical measurement setup in the lab at their site in Austin and offered the student assistance on paper writing.

- M. Kazdagli, **V. Janapa Reddi**, M. Tiwari. "Quantifying and Improving the Efficiency of Hardware-based Mobile Malware Detectors," in IEEE International Symposium on Microarchitecture (MICRO), October 2016 (Accepted).
  - A. Co-authors:
    - i. M. Kazdagli — The University of Texas at Austin, Dr. Tiwari's student
    - ii. V. Janapa Reddi — The University of Texas at Austin
    - iii. M. Tiwari — The University of Texas at Austin, ECE faculty
  - B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the majority of the work, with my assistance as a co-advisor both of the intellectual content and of the written work. I contributed the intellectual material associated with the mobile computing part of research article, while Prof. M. Tiwari, who is the lead advisor, for the student guided the student on the security aspects of the research which is the primary focus of the article.

- N. Chachmon, D. Richins, R. Cohn, M. Christensson, W. Cui, **V. Janapa Reddi**. "Simulation and Analysis Engine for Scale-out Workloads," in IEEE International Conference on Supercomputing (ICS), June 2016. http://dx.doi.org/10.1145/2925426.2926293
  - A. Co-authors:
    - i. N. Chachmon — Intel Corporation
    - ii. D. Richins — The University of Texas at Austin, my student
    - iii. R. Cohn — Intel Corporation
    - iv. M. Christensson — Intel Corporation
    - v. W. Cui — The University of Texas at Austin, my student
    - vi. V. Janapa Reddi — The University of Texas at Austin
  - B. Qualitative statement of contribution: my students performed the majority of the work in crafting the research article, but the first author is an Intel author because the work was predominantly built out of Intel before my students got involved in the research. I provided assistance as a co-

advisor to the entire team both of the intellectual content and of the written work.

- Y. Liu, Z. Yu, L. Eeckhout, **V. Janapa Reddi**, Y. Luo, X. Wang, Z. Wang, C. Xu. "Barrier-Aware Warp Scheduling for Throughput Processors," in IEEE International Conference on Supercomputing (ICS), June 2016. http://dx.doi.org/10.1145/2925426.2926267
  A. Co-authors:
     i. Y. Liu — Peking University
     ii. Z. Yu — Shenzhen Institute of Advanced Technology, CAS
     iii. L. Eeckhout — Ghent University
     iv. V. Janapa Reddi — University of Texas at Austin
     v. Y. Luo — Peking University
     vi. X. Wang — Peking University
     vii. Z. Wang — Michigan Tech University
     viii. C. Xu — Shenzhen Institute of Advanced Technology, CAS
  B. Qualitative statement of contribution: I provided assistance as an expert on GPU architectures on both the intellectual content and the written work.

- Y. Zhu, **V. Janapa Reddi**. "GreenWeb: Language Extensions for Energy Efficient Mobile Web Computing," in ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2016. http://dx.doi.org/10.1145/2908080.2908082
  A. Co-authors:
     i. Y. Zhu — The University of Texas at Austin, my student
     ii. V. Janapa Reddi — The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- M. Halpern, Y. Zhu, **V. Janapa Reddi**. "Mobile CPU's Rise to Power: Quantifying the Impact of Generational Mobile CPU Design Trends on Performance, Energy, and User Satisfaction" in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.64-76, March 2016. http://dx.doi.org/10.1109/hpca.2016.7446054
  A. Co-authors:
     i. M. Halpern — The University of Texas at Austin, my student
     ii. Y. Zhu — The University of Texas at Austin, my student
     iii. V. Janapa Reddi — The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- Y. Zhu, D. Richins, M. Halpern, **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Server-side Web Applications," in IEEE International Symposium on Microarchitecture (MICRO), pp.762-774, December 2015. http://dx.doi.org/10.1145/2830772.2830792
  A. Co-authors:
     i. Y. Zhu — The University of Texas at Austin, my student
     ii. D. Richins — The University of Texas at Austin, my student
     iii. M. Halpern — The University of Texas at Austin, my student
     iv. V. Janapa Reddi — The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- Y. Zu, C. R. Lefurgy, J. Leng, M. Halpern, M. S. Floyd, **V. Janapa Reddi**. "Adaptive Guardband Scheduling to Improve System-level Efficiency of the POWER7+," in IEEE International Symposium on Microarchitecture (MICRO), pp.308-321, December 2015. http://dx.doi.org/10.1145/2830772.2830824
  A. Co-authors:
     i. Y. Zu — The University of Texas at Austin
     ii. C. R. Lefurgy — IBM

iii. J. Leng — The University of Texas at Austin, my student
iv. M. Halpern — The University of Texas at Austin, my student
v. M. S. Floyd — IBM
vi. V. Janapa Reddi — The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work. The IBM co-authors provided access to IBM POWER7+ server and helped with IBM's software toolchain used for the research and they also offered assistance in developing the paper.

- J. Leng, A. Buyuktosunoglu, R. Bertran, P. Bose, **V. Janapa Reddi**. "Safe Limits on Voltage Reduction Efficiency in GPUs: a Direct Measurement Approach," in IEEE International Symposium on Microarchitecture (MICRO), pp.294-307, December 2015. http://dx.doi.org/10.1145/2830772.2830811

A. Co-authors:

i. J. Leng — The University of Texas at Austin and IBM, my student
ii. A. Buyuktosunoglu — IBM T.J. Watson Research Center
iii. R. Bertran — IBM T.J. Watson Research Center
iv. P. Bose — IBM T.J. Watson Research Center
v. V. Janapa Reddi — The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work. The IBM co-authors provided access to physical measurement setup in the lab at their site in Austin and offered the student assistance on paper writing.

- M. Halpern, Y. Zhu, R. Peri, **V. Janapa Reddi**. "Mosaic: Cross-Platform User-Interaction Record and Replay for The Fragmented Android Ecosystem," in IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), pp.215-224, March 2015. http://dx.doi.org/10.1109/ispass.2015.7095807

A. Co-authors:

i. M. Halpern — The University of Texas at Austin, my student
ii. Y. Zhu — The University of Texas at Austin, my student
iii. R. Peri — Intel Corporation
iv. V. Janapa Reddi — The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work. The Intel co-author provided access to physical measurement setup in the lab at their site in Austin that we used to develop the original research contributions.

- Y. Zhu, M. Halpern, **V. Janapa Reddi**. "Event-based Scheduling for Energy-Efficient Quality of Service (eQoS) in Mobile Web Applications," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.137-149 February 2015. http://dx.doi.org/10.1109/hpca.2015.7056028

A. Co-authors:

i. Y. Zhu — The University of Texas at Austin, my student
ii. M. Halpern — The University of Texas at Austin, my student
iii. V. Janapa Reddi — The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- J. Leng, Y. Zu, **V. Janapa Reddi**. "GPU Voltage Noise: Characterization and Hierarchical Smoothing of Spatial and Temporal Voltage Noise Interference in GPU Architectures," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.161-173, February 2015. http://dx.doi.org/10.1109/hpca.2015.7056030

A. Co-authors:

i. J. Leng — The University of Texas at Austin, my student
ii. Y. Zu — The University of Texas at Austin, my student
iii. V. Janapa Reddi — The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- J. Leng, Y. Zu, M. Rhu, M. Gupta, **V. Janapa Reddi**. "GPUVolt: Modeling and Characterizing Voltage Noise in GPU Architectures," in IEEE International Symposium on Low Power Electronics and Design (ISLPED), pp.141-146, August 2014. http://dx.doi.org/10.1145/2627369.2627605
  A. Co-authors:
     i. J. Leng — The University of Texas at Austin, my student
     ii. Y. Zu — The University of Texas at Austin, my student
     iii. M. Rhu — The University of Texas at Austin, my student
     iv. M. Gupta — IBM T.J. Watson, Ossining, NY.
     v. V. Janapa Reddi — The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work. The IBM collaborator provided her industrial expertise on power modeling. Her input was valuable in making sure the models were representative of industry trends.

- C. Zhou, X. Wang, W. Xu, Y. Zhu, **V. Janapa Reddi**, C. Kim, "Estimation of Instantaneous Frequency Fluctuation in a Fast DVFS Environment Using an Empirical BTI Stress-Relaxation Model," in IEEE International Symposium on International Reliability Physics Symposium (IRPS), pp.2D.2.1-2D.2.6, June 2014. http://dx.doi.org/10.1109/irps.2014.6860593
  A. Co-authors:
     i. C. Zhou — The University of Minnesota
     ii. X. Wang — The University of Minnesota
     iii. W. Xu — The University of Minnesota
     iv. Y. Zhu — The University of Texas at Austin, my student
     v. V. Janapa Reddi — The University of Texas at Austin
     vi. C. Kim — The University of Minnesota
  B. Qualitative statement of contribution: my student and I helped our co-authors with the paper both in intellectual capacity and in developing the research article. My student helped with the mobile device measurement setup, and I provided assistance as an advisor both of the intellectual content and of the written work.

- Y. Zhu, **V. Janapa Reddi**. "WebCore: Architectural Support for Interactive Mobile Web Browsing," in ACM/IEEE International Symposium on Computer Architecture (ISCA), pp.541-552, June 2014. http://dx.doi.org/10.1109/isca.2014.6853239
  A. Co-authors:
     i. Y. Zhu — The University of Texas at Austin, my student
     ii. V. Janapa Reddi — The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- J. Leng, T. Hetherington, A. ElTantawy, S. Gilani, N. Kim, T. Aamodt, **V. Janapa Reddi**. "GPUWattch: Enabling Energy Optimizations in GPGPUs," in ACM/IEEE International Symposium on Computer Architecture (ISCA), vol 41(3), pp.487-498, June 2013. http://dx.doi.org/10.1145/2485922.2485964
  A. Co-authors:
     i. J. Leng — The University of Texas at Austin, my student
     ii. T. Hetherington — University of British Columbia
     iii. A. ElTantawy — University of British Columbia
     iv. S. Gilani — University of Wisconsin-Madison
     v. N. Kim — University of Wisconsin-Madison
     vi. T. Aamodt — University of British Columbia
     vii. V. Janapa Reddi — The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my overall assistance as an advisor both of the intellectual content and of the written work. I was the team leader for this multi-institution effort as the work started at UT Austin and our collaborators were sought out for their unique expertise. In addition to leadership, I provided technical expertise to power measurement and modeling.

- Y. Zhu, **V. Janapa Reddi**. "High-Performance and Energy-Efficient Mobile Web Browsing on Big/Little Systems," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.13-24, February 2013. http://dx.doi.org/10.1109/hpca.2013.6522303
  A. Co-authors:
     i. Y. Zhu — The University of Texas at Austin, my student
     ii. V. Janapa Reddi — The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the student performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- **V. Janapa Reddi**, D. Pan, S. Nassif, K. Bowman. "Robust and Resilient Designs from the Bottom Up: Technology, CAD, Circuit, and System Issues," in IEEE International Symposium on Asia and South Pacific Design Automation Conference (ASP-DAC), pp.7-16 June 2012. http://dx.doi.org/10.1109/aspdac.2012.6165064
  A. Co-authors:
     i. V. Janapa Reddi — The University of Texas at Austin
     ii. D. Pan — The University of Texas at Austin
     iii. S. Nassif — IBM
     iv. K. Bowman — Intel Corporation
  B. Qualitative statement of contribution: This was an invited article and all authors contributed equally to the insights and future directions that are outlined in the work. I led the paper.

- S. Campanoni, T. Jones, G. Holloway, **V. Janapa Reddi**, G. Wei, D. Brooks, "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing," in IEEE/ACM International Symposium on Code Generation and Optimization (CGO), pp.84-93, March, 2012. http://dx.doi.org/10.1145/2259016.2259028
  A. Co-authors:
     i. S. Campanoni — Harvard University, Cambridge
     ii. T. Jones — University of Cambridge, Cambridge
     iii. G. Holloway — Harvard University, Cambridge
     iv. V. Janapa Reddi — The University of Texas at Austin
     v. G. Wei — Harvard University, Cambridge
     vi. D. Brooks — Harvard University, Cambridge
  B. Qualitative statement of contribution: this is part of the first author's postdoctoral research; the postdoc performed the majority of the work, with my partial assistance as an advisor both of the intellectual content and of the written work. I contributed to the writing of the article and the intellectual ideas that went into the development of the compiler.

- **V. Janapa Reddi** and D. Brooks. "Resilient Architectures via Collaborative Design: Maximizing Commodity Processor Performance in the Presence of Variations," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 30(10), pp.1429-1445, October 2011. http://dx.doi.org/10.1109/tcad.2011.2163635
  A. Co-authors:
     i. V. Janapa Reddi — The University of Texas at Austin
     ii. D. Brooks — Harvard University, Cambridge
  B. Qualitative statement of contribution: this was an invited article and I did all of the writing and the research that went into the article.

B. Refereed Journal Publications (8 Papers)

- Y. Zhu, M. Halpern, **V. Janapa Reddi**. "The Role of the CPU in Energy-Efficient Mobile Web Browsing," in IEEE MICRO — Special issue on Mobile Systems, vol. 35(1), pp. 26-33, January 2015. http://dx.doi.org/10.1109/mm.2015.8
  - A. Co-authors:
    - i. Y. Zhu — The University of Texas at Austin, my student
    - ii. M. Halpern — The University of Texas at Austin, my student
    - iii. V. Janapa Reddi — The University of Texas at Austin
  - A. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- Y. Zhu, A. Srikanth, J. Leng, **V. Janapa Reddi**. "Exploiting Webpage Characteristics for Energy-Efficient Mobile Web Browsing," in IEEE Computer Architecture Letters (CAL), pp.33-36, October 2012. http://dx.doi.org/10.1109/l-ca.2012.33
  - A. Co-authors:
    - i. Y. Zhu — The University of Texas at Austin, my student
    - ii. A. Srikanth — The University of Texas at Austin, my student
    - iii. J. Leng — The University of Texas at Austin, my student
    - iv. V. Janapa Reddi — The University of Texas at Austin
  - B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Mobile Processors for Energy-Efficient Web Search," in ACM Transactions on Computer Systems (TOCS), vol 29(3), art.9, August 2011. http://dx.doi.org/10.1145/2003690.2003693
  - A. Co-authors:
    - i. V. Janapa Reddi — The University of Texas at Austin
    - ii. B. Lee — Duke University, Durham, NC
    - iii. T. Chilimbi — Microsoft Research
    - iv. K. Vaid — Microsoft Corporation
  - B. Qualitative statement of contribution: this was work that I spearheaded with my co-authors. I am responsible for its intellectual contributions. My co-authors were invaluable in shaping the contributions and also in developing the content that we agreed to include the write-up.

D. Workshops (10 Papers)

- M. Kazdagli, L. Huang, **V. Janapa Reddi**, M. Tiwari. "Morpheus: Benchmarking Computational Diversity in Mobile Malware," in Workshop on Hardware and Architectural Support for Security and Privacy. June 2014. http://dx.doi.org/10.1145/2611765.2611767
  - A. Co-authors:
    - i. M. Kazdagli — University of Texas at Austin, Dr. Tiwari's student
    - ii. L. Huang — Intel Corporation
    - iii. V. Janapa Reddi — University of Texas at Austin
    - iv. M. Tiwari — University of Texas at Austin
  - C. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the student performed the majority of the work, with my assistance as a co-advisor both of the intellectual content and of the written work. The lead advisor is Prof. M. Tiwari. My assistance was on the mobile computing aspects, specifically involving CPU and SoC performance measurements. The crux of the security work and advisory on that fell upon Dr. L. Huang and Prof. M. Tiwari.

- S. Chai, D. Zhang, J. Leng, **V. Janapa Reddi**. "Lightweight Detection and Recovery Mechanisms to Extend Algorithm Resiliency in Noisy Computation," in Workshop on Near-threshold Computing (co-located with ISCA), June 2014
  - A. Co-authors:
    - i. S. Chai — SRI International

ii. D. Zhang SRI International
iii. J. Leng The University of Texas at Austin, my student
iv. V. Janapa Reddi The University of Texas at Austin

B. Qualitative statement of contribution: this is part of the student's Ph.D. research; the student performed the work over an internship at SRI during which I was involved as the student's advisor. I provided assistance in steering the research direction, and in addition I provided intellectual ideas and feedback on algorithmic resiliency based on my compiler background and expertise.

- J. Leng, Y. Zu, **V. Janapa Reddi**. "Energy Efficiency Benefits of Reducing the Voltage Guardband on the Kepler GPU Architecture," in IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE). March 2014.
  A. Co-authors:
     i. J. Leng The University of Texas at Austin, my student
     ii. Y. Zu The University of Texas at Austin, my student
     iii. V. Janapa Reddi The University of Texas at Austin
  B. Qualitative statement of contribution: this is part of the first student's Ph.D. research; the students performed the majority of the work, with my assistance as an advisor both of the intellectual content and of the written work.

- L. Guckert, M. O' Connor, S. Ravindranath, Z. Zhao, **V. Janapa Reddi**. "A Case for Persistent Caching of Compiled JavaScript Code in Mobile Web Browsers," in Workshop on Architectural and Microarchitectural Support for Binary Translation. March 2013.
  A. Co-authors:
     i. L. Guckert The University of Texas at Austin, student from my class
     ii. M. O' Connor The University of Texas at Austin, student from my class
     iii. S. Ravindranath The University of Texas at Austin, student from my class
     iv. Z. Zhao The University of Texas at Austin, student from my class
     v. V. Janapa Reddi The University of Texas at Austin
  B. Qualitative statement of contribution: this work was the product of a class project. I provided the students with my assistance as an advisor both of the intellectual content and of the written work.

- S. Kanev, T. M. Jones, G. Wei, D. Brooks, **V. Janapa Reddi**. "Measuring Code Optimization Impact on Voltage Noise," in IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE). March 2013.
  A. Co-authors:
     i. S. Kanev Harvard University
     ii. T. M. Jones Harvard University
     iii. G. Wei Harvard University
     iv. D. Brooks Harvard University
     v. V. Janapa Reddi The University of Texas at Austin
  B. Qualitative statement of contribution: this was the product of a research undergraduate that I was mentoring, who happened to be at Harvard at the time the article was written; the student performed the majority of the work, with my assistance as a co-advisor both of the intellectual content and of the written work.

Section 2. Works published (or in equivalent status) while in current rank at other institutions (if applicable)

Not applicable.

Section 3. Works published (or in equivalent status) while in previous rank(s) at UT Austin (if applicable)

Not applicable.

Section 4. Works published (or in equivalent status) while in previous rank(s) at other institutions (if applicable)

Not applicable.

C33

Subject: [MICRO49] Accepted paper #93 "Ti states: Processor Power Management in..."
From: <micro49pcchairs@gmail.com>
Date: Sat, 25 Jun 2016 21:38:15 +0800
To: Indrani Paul <Indrani.Paul@amd.com>, Vijay Janapa Reddi <vj@ece.utexas.edu>, Wei Huang <WeiN.Huang@amd.com>, Yazhou Zu <yazhou.zu@utexas.edu>
CC: Hsien-Hsin Sean Lee <micro49pcchairs2@gmail.com>

Dear authors,

The the 49th ACM/IEEE International Symposium on Microarchitecture (MICRO49) program committee is delighted to inform you that your paper #93 has been accepted to appear in the conference.

Title: Ti states: Processor Power Management in the Temperature Inversion Region
Authors: Yazhou Zu (University of Texas at Austin)
Wei Huang (AMD Research)
Indrani Paul (AMD Research)
Vijay Janapa Reddi (University of Texas at Austin)
Paper site: http://micro49submit.csie.org/paper.php/93?cap=093alh49GN0iLDc

Your paper was one of 61 accepted out of 283 submissions. Congratulations!

Reviews and comments on your paper are appended to this email. The submissions site also has the paper's reviews and comments, as well as more information about review scores.

Camera-ready versions of your paper must be uploaded to the submission web site by August 1, 2016. Please do your best to address the reviewer comments as you revise your paper.

Contact Hsien-Hsin Sean Lee <micro49pcchairs2@gmail.com> with any questions or concerns.

- MICRO49 Submissions

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MICRO49 Review #93A

Paper #93: Ti states: Processor Power Management in the Temperature Inversion Region

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Overall merit: 7. Strong accept
Reviewer expertise: 3. Knowledgeable
Novelty: 4. Surprisingly new contribution
Writing quality: 4. Well-written

===== Paper summary =====

The paper takes advantage of temperature inversion phenomenon in which increase in transistor temperature improves the transistor delay when it operates at a certain voltage region. The phenomenon allows adaptive margining by reducing the supply voltage to save power in temperature inversion region while running transistors at the same performance point set by the design. Thermal and voltage characterisation has been done on AMD chips having CPUs+GPUs. Workload-based characterisation is performed to create a table of temperatures and voltage setting pair to find near-optimal operating voltage for different temperatures.

C34

Subject: [MICRO49] Accepted paper #248 "Quantifying and Improving the Efficiency..."
From: <micro49pcchairs@gmail.com>
Date: Sat, 25 Jun 2016 21:38:16 +0800
To: Mikhail Kazdagli <mikhail.kazdagli@utexas.edu>, Mohit Tiwari <tiwari@austin.utexas.edu>, Vijay Janapa Reddi <vj@ece.utexas.edu>
CC: Hsien-Hsin Sean Lee <micro49pcchairs2@gmail.com>

Dear authors,

The the 49th ACM/IEEE International Symposium on Microarchitecture (MICRO49) program committee is delighted to inform you that your paper #248 has been accepted to appear in the conference.

Title: Quantifying and Improving the Efficiency of Hardware-based Mobile Malware Detectors
Authors: Mikhail Kazdagli (University of Texas at Austin)
Vijay Janapa Reddi (University of Texas at Austin)
Mohit Tiwari (University of Texas at Austin)
Paper site: http://micro49submit.csie.org/paper.php/248?cap=0248azE6CCLtiGGE

Your paper was one of 61 accepted out of 283 submissions. Congratulations!

Reviews and comments on your paper are appended to this email. The submissions site also has the paper's reviews and comments, as well as more information about review scores.

Camera-ready versions of your paper must be uploaded to the submission web site by August 1, 2016. Please do your best to address the reviewer comments as you revise your paper.

Contact Hsien-Hsin Sean Lee <micro49pcchairs2@gmail.com> with any questions or concerns.

- MICRO49 Submissions

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MICRO49 Review #248A

Paper #248: Quantifying and Improving the Efficiency of Hardware-based Mobile Malware Detectors

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Overall merit: 6. Accept
Reviewer expertise: 3. Knowledgeable
Novelty: 3. New contribution
Writing quality: 3. Adequate

===== Paper summary =====

The paper proposes hardware malware detector for mobile platforms. The paper presents two unsupervised HMDs, namely bag of words and markov model based anomaly detector. The paper also presents the notion of app-specific HMDs.

===== Strengths =====

The paper presents a good direction for future security in mobile malware detection space, namely Hardware detectors. The paper presents improvement techniques to supervised and unsupervised HMDs and offers the operating range

Janapa Reddi

Budget Council Assessment on Teaching for Faculty Promotion Candidate Vijay Janapa Reddi

This statement on teaching for Assistant Professor Vijay Janapa Reddi was prepared by Budget Council Member Professor Jonathan Valvano. The statement was prepared following a review of his course evaluations, reading/evaluating his teaching portfolio, in class observations made by Professors John, Chiou, and Alù, discussions with Professor Janapa Reddi, interviews with students in his EE319K, and an in-depth knowledge of ECE departmental activities.

Principal Areas of Teaching
Dr. Janapa Reddi's principal area of teaching is in computer engineering in general and architecture and embedded systems in specific. As an assistant professor he has taught three different courses: a lower division required undergraduate class and two advanced graduate classes.

Teaching Evaluation Procedures and Measures
The department uses course evaluation surveys and peer evaluations. It is normal practice to conduct official course evaluations at the conclusion of every class. However, there was a miscommunication Spring 2015 over whether EE319K was to have paper or online evaluations, and unfortunately the official EE319K survey for Spring 2015 was not performed. In spring semesters, EE319K is a large enrollment class with 5 sections. I was one of the instructors Spring 2014, Spring 2015, and Spring 2016 along with Professor Janapa Reddi. Since we have shared homework, shared labs and shared exams, I can attest that Professor Janapa Reddi's students were well-taught each of these three semesters. I think the teaching evaluations for Spring 2014 and Spring 2016 capture an accurate representation of his EE319K teaching, and the missing Spring 2015 evaluation data is not of concern.

Peer evaluations are conducted nominally once per academic year. Peer evaluations are made by tenured professors after a visit to the classroom. The times and dates of these visits are agreed to beforehand so that there are no surprise visits.

- Professor John observed EE382V, Dynamic Compilation on April 30, 2012
- Professor Chiou observed EE382V, Dynamic Compilation on April 29, 2013
- Professor John observed EE319K, Embedded Systems on April 17, 2014
- Professor Chiou observed EE382N-10, Parallel Architecture on Nov 30, 2015
- Professor Alù visited EE 319K, Embedded Systems, on March 28, 2016

The November 2015 observation was an invited guest lecture that Professor Janapa Reddi gave to Professor Chiou's class.

Summary of Teaching Evaluations
The main indicator on the Course Evaluation Surveys used to evaluate teaching performance is the Overall Instructor Rating. His in rank instructor ratings are summarized in Table 1. The GPA for EE319K, the undergraduate required class, is

purposely adjusted to be about 3.0 for all sections. Also this GPA is consistent with other classes at this level. Therefore, I believe there is no bias in evaluation scores caused by perceived grade expectations. The average size for graduate classes in ECE has been 17.6 students. The average size of his graduate class is 17.8 students, approximately equal to the department average.

His weighted average undergraduate instructor rating is 4.35 out of 5, and his weighted average graduate rating is 4.30 out of 5. His performance is above the department average for undergraduate courses (ECE weighted average = 4.17) and slightly below the department average for graduate courses (ECE weighted average = 4.45). In summary, his undergraduate and graduate instructor ratings are consistently excellent.

Semester	Course	#Enrolled / #Answered	Overall instructor rating	Overall course rating
Spring 2014	EE 319K	35/68	**4.4**	4.2
Spring 2015	EE 319K	missed		
Spring 2016	EE 319K	35/68	**4.3**	4.0
Fall 2015	EE 382V Code Generation	29/26	**4.4**	4.0
Fall 2012	EE 382V Code Generation	16/13	**4.5**	4.2
Fall 2014	EE 382V Dynamic Compilation	15/12	**4.3**	4.1
Spring 2013	EE 382V Dynamic Compilation	8/8	**4.4**	4.1
Spring 2012	EE 382V Dynamic Compilation	21/19	**4.0**	3.4

Table 1. CIS results for undergraduate and graduate teaching.

I interviewed his EE319K students on May 13th 2016

"Enthusiastic"
"Into teaching"
"He takes initiative to introduce new topics"
"He makes you figure it out. He makes you learn"
"He could slow down"
"He teaches you to learn. He encourages you to go beyond the class"

"I learned a lot more than what was in the lab or the exams"
"During his lectures he would incorporate issues engineers have to consider"
"He forced me to think outside the box"
"Awesome"
"Very passionate about the subject"

Peer Comparison and Summary

One way to evaluate Professor Janapa Reddi is to compare his teaching to the other professors who taught EE 319K during this time, see Table 2. Five of the six professors teaching EE319K also have excellent CIS scores, and Professor Janapa Reddi is one of our best EE319K instructors. The weighted average instructor CIS score for this course is 4.37 and the weighted average course CIS score is 4.02. These averages are above the department, college and university averages, signifying EE319K is an effective educational experience for the students.

	Average		Average
CIS Instructor	4.35	CIS Instructor	4.05
CIS Course	4.10	CIS Course	3.90
CIS Instructor	2.80	CIS Instructor	4.00
CIS Course	3.20	CIS Course	4.00
CIS Instructor	4.55	CIS Instructor	4.66
CIS Course	4.05	CIS Course	4.10

Table 2. CIS data in rank of all EE 319K instructors (source: CIS). Professor Janapa Reddi's data is highlighted.

Response to Student and Peer Evaluation Leads to Continuous Improvement

There are not a lot of negative comments about Professor Janapa Reddi's teaching, but one theme that exists is his quick pace. Both peer review and student evaluations suggest he reduce the speed of delivery. During the Spring 2016 semester he interjected stopping points in his lectures to allow students to ask more questions. This style was positively received by his students.

One of the difficult concepts in EE319K is teaching C programming to students with no prior programming experience other than EE306/BME303. Basically the problem is there are some students with extensive programming experience and others who just have this one prerequisite class (EE306/BME303) on assembly programming and computer architecture. Student evaluations point to this fact as one of the difficult problems to overcome in EE319K. Rather than blasting students with a lot of details, Professor Janapa Reddi tried to focus on the fundamental process of software design in C. His students appreciated his desire to make them think and to make them understand what they were building.

Janapa Reddi

Summarizing quotes from Professor John's in class visit. April 30, 2012

Dr. Janapa Reddi delivered a lecture on Reliability Wall and explained how hardware software co-design is important. The content of the lecture was clear to the students. Relevancy of the main ideas was clear in the presentation. Students interacted with the instructor during the lecture. Out of the 20 students in the class, more than 10 asked questions. Many asked multiple questions.

The visual aids were good. Dr. Reddi used Power Point slides. They were clear and could be easily read from the back of the class. The slides were effective. Dr. Reddi appeared confident and enthusiastic.

Overall, Dr. Reddi delivered a good lecture. But it would be worthwhile to visit an undergraduate class taught by Dr. Reddi in the future, so one could evaluate his teaching ability for more basic material.

Summarizing quotes from Professor Chiou's in class visit. April 29, 2013

It was very clear that the students enjoyed being in the class, and were very engaged throughout. Vijay embeds questions into the slides, letting him know when to pause and ask the question. I think that's a very effective way to let the students know when there was a major point and they can think about the question and its answer as Vijay is lecturing on the topic. There were a lot of questions in addition to those embedded questions. Vijay is very passionate about the subject material and it shows.

The pace was fast, and very fast during an introduction to a topic, but it was clear that the introduction was simply a summary of what had been covered before. Once he got to the new material he was still fast, but the questions coming from the students clearly indicated that the pace was fine for them. I think had the class had weaker students, it would be too fast, but I think for this particular set of students, it was fine. I know many of the students in his class, who are some of the very best students in our department.

Vijay's teaching methods were very effective and appropriate for this class. He may be too fast for a weaker class, but I think he had tuned his pace for this particular set of students. There was a lot of material covered, probably too much if it was a normal lecture, but this was partially a review for the oral exam. Some of the text on the slides could be a bigger.

Summarizing quotes from Professor John's in class visit. April 17, 2014

Dr. Janapa Reddi delivered a lecture on embedded systems interfacing and programming, especially on bitmap file format for images. The content was presented clearly. He spoke loudly and clearly. He asked several questions to students and the students responded well. He described the lab assignment and had a demonstration of some relevant lab material. There were about 50 students in the class. They were attentive. Dr. Reddi was able to capture their attention and interest.

Dr. Reddi appeared well-prepared. The visual aids were good. Dr. Reddi used Power Point slides. They were clear and could be easily read from the back of the class. The slides were effective. Dr. Reddi walked around in the class and interacted with the students. Dr. Reddi appeared confident and enthusiastic. He seemed passionate about teaching.

Overall, Dr. Reddi delivered an excellent lecture. I had visited a graduate class of Dr. Reddi in an earlier year. The undergraduate teaching was even better than his graduate teaching. I do not have any concerns on his teaching.

Summarizing quotes from Professor Chiou's in class visit. Nov 30, 2015

Vijay has a lot of passion when he teaches. He is very engaging and animated. He moves around the classroom and uses the boards that are available effectively. It is very clear that he knows the material very well. He understands questions and answers them effectively, providing the right amount of detail. He gave a nice summary at the end of the lecture.

It would have been good to have something to point students to that they could look at right after class. He is describing something new that is not fully available, however, so it is understandable that he could not provide that at this time.

The students are paying attention and engaged.

His speed is a bit too quick on overview material, which probably reduced the number of questions somewhat during that part of the lecture. He got a lot more questions as he slowed down towards the end of the class.

In terms of areas to improve, I would say slow down a bit and ask the class a few more questions during the new material. It might help to slightly reduce the amount of material to be covered.

Overall, the class went very well. I personally learned something very useful today.

Summarizing quotes from Professor Alù's in class visit. March 28, 2016

The lecture was focused on the preparation for an upcoming midterm exam, and focused on several problems, in line with what the exam was expected to focus on. The lecture was well introduced and well prepared, the discussion was clear and linear, the examples were well organized and drew the attention of most of the class. Students were able to follow the pace and were in average quite engaged, probably as much as it can be expected in a lower-level required EE course. Explanations were clear and at a good pace. Questions and comments from students were answered clearly, at a good level and with sufficient length. Prof. Reddi encouraged questions and clearly answered them throughout the class, and the atmosphere was very positive.

Writing may be in some instances difficult to follow, especially from the back of the class, where some students may lose attention. This may be improved by using a larger font on the board. In any case, this issue is mostly due to facilities: the large auditorium, with seats relatively far from the projector screen and the blackboard, does not help.

Class involvement may be improved by trying to engage the students sitting in the back. Prof. Reddi gave several opportunities during class to ask questions and comments, and answered very clearly, engaging the class, but the students in the back rows appeared less involved.

The end of class was quite abrupt, it may be used to summarize the discussion and introduce next topics.

Janapa Reddi

Teaching Portfolio
There are three aspects of Professor Janapa Reddi's teaching portfolio that demonstrate he is an effective and passionate educator. First, it is clear he prepares for class with the creation of slides and handouts. Second, he is willing to adapt his class to specific needs of his students. His "codefest" in EE319K was in response to students having trouble programming in C. Third, he is open to trying new approaches to education. Some of these approaches involve teaching style (hands on learning), others involve homework and lab assignments, and others involve examinations.

Describe participation on graduate committees
Professor Janapa Reddi has one PhD student who passed the defense and is expected to graduate Dec 2016. He has one PhD student in candidacy. He has four other PhD-bound students in the pipeline. He supervised 2 MS thesis students in rank that have graduated (one is co-supervised). In addition to his students, he has served or is serving on 9 PhD committees.

Conclusions
According to his teaching portfolio, the key tenet of his "teaching philosophy is hands-on learning." It is clear from all accounts that Professor Janapa Reddi combines the passion and the skills to be an effective educator. Professor Janapa Reddi was given the opportunity to teach a more advanced undergraduate class, but choose to further develop his undergraduate teaching skills by teaching EE319K a third time. His desire is to make an educational impact outside the 40 acres. Thus, he has been quite active in K-12 outreach, creating a hands-on computer science class using Arduino for 5th and 6th graders. In conclusion, in all areas of teaching (outreach, undergraduate, and graduate), Professor Janapa Reddi demonstrates the excellence that clearly supports this promotion.

Summary prepared by Budget Council Member Professor Jonathan Valvano.

Jonathan Valvano

Jonathan Valvano

Teaching Statement

Vijay Janapa Reddi

1 Introduction

My teaching effort spans a broad spectrum of activities that I have developed over recent years and continue to actively refine on a regular basis. These activities involve curriculum development and enhancement, K-12 outreach programs that have become mainstream into the Austin Independent School District (AISD), and the development of new technology based on wearable devices to build a smarter, future classroom.

A key tenet of my teaching philosophy is hands-on learning. Modern-day computer systems are complex. Traditional pedagogical teaching cannot fully convey the overwhelming complexity of these systems and the need for principled design approaches, not just within one layer of the system stack, but across the different layers of the system stack. Hands-on learning based on exploration and using real-world software and hardware, however, can bridge the growing void between pedagogical teaching and real systems.

2 Undergraduate Curriculum Development: Relevance and Open-Source Technology

Over the past five years, I have been improving our introduction to the embedded systems course (EE319k) that is taught at the freshman level through a hands-on learning approach. The course is designed to help students understand the relationship and interaction between computer science (i.e., software) and electrical engineering (i.e., hardware). Students learn C and assembly programming to control general- and special-purpose I/O pins on a microcontroller board to perform specific tasks. The course culminates with a project in which students demonstrate the skills they have acquired through creative and open-ended group projects. It is a very important course because it is where students first get exposure to a real system.

I am greatly interested in helping such important and traditional courses at UT become more relevant to students by introducing state-of-the-art embedded systems and mobile computing platforms into the class. Embedded systems have evolved from simple microcontroller-based platforms to general-purpose computers capable of intelligent data processing. Thus, there is opportunity to make the class relevant to current times. I have begun taking steps to transform the class by introducing discussion about active sensors (e.g., accelerometers) as input and output peripherals, rather than relying only on passive components (e.g., switches and resistors). In practice, I have found that when students use active sensors in the class, their learning interest and creativity improves significantly. Keeping students engaged and interested allows me to teach students the elements of computing far more deeply. Moreover, it facilitates self-learning.

Overall, *my course evaluations for EE319k have been strong.* I have received instructor ratings of 4.4 out of 5, which is above the university average (4.2). I believe that the strong evaluations are the result of me making an effort to improve. Over the course of the semester, I ask for candid and anonymous written feedback from students so that I can reform my teaching style as the semester progresses—every class is unique, and so I do my best as the instructor to adapt to the needs of my different students in the class. Over the years, I have noticed that the number of students that are actively seeking to take my section (out of many) has increased. I believe that this is due to me slowly but steadily becoming better at helping students learn.

Looking forward, I want to improve EE319k by replacing the microcontroller-based platform we use today with a more general-purpose computing system such as the Raspberry Pi. The Raspberry Pi will facilitate a graceful transition to teaching students more advanced principles of a general-purpose computing system without losing focus on the Advanced RISC Machine (ARM) Instruction Set Architecture (ISA), which is widely adopted by the embedded and mobile computing industry and as such it is essential for our students to comprehend it fully. The Raspberry Pi could serve as a stable ARM ISA based platform for teaching advanced classes in the later years, such as operating systems, compilers and software engineering. Having a consistent platform for all the classes greatly reduces the burden on the instructors

and students to continuously learn new infrastructures, and instead allow for more time on teaching and learning. Furthermore, since working with the Raspberry Pi does not require any proprietary software, students can continue to explore learning on their own (i.e., post-class). They can make use of the open-source software and online lessons available on the Web, thus paving the way for continuous and open learning.

3 Graduate Teaching: New Classes with Focus on Practicality and Industry Relevance

My passion is to teach courses that fall at the intersection of hardware and software. In this general genre, I have experience teaching two different types of compiler courses and one virtual machines course. In addition, as previously described, I teach introduction to embedded systems at the undergraduate level, which yet again reinforces the important relationship between the hardware and software layers. My course evaluation scores have consistently been above UT Austin's average, ranging between 4.3 and 4.5 out of 5.

Code Generation and Optimization (CGO): I teach a compilers course at the graduate level that is also taken by undergraduate students. The course introduces students to the basics of code generation and optimization on x86 platforms. Students use the industry-strength LLVM compiler for class assignments and projects because it is important for them to work with production-grade open-source tools.

The unique twist in my version of the compilers course is its focus on the compiler 's symbiosis with hardware. Students learn how compilers and the processor architecture interact with one another. I emphasize how design-time hardware decisions are made based on compiler capabilities, and vice versa. For instance, students learn the differences, challenges, and opportunities in code generation and optimization for an out-of-order processor versus a VLIW processor. I also emphasize how optimizations performed at the compiler and hardware level either work in conjunction or can conflict with one another, such as in the case of instruction scheduling at the compiler versus at the hardware level in an out-of-order processor.

Students graduate with an intense understanding of the complex yet symbiotic relationship between hardware and software. The shortcoming, however, is that students need to take more compiler courses to understand program analysis—compilers are complex, and cannot be fully covered by any one course.

Dynamic Compilation/Virtual Machines: Complementary to the CGO course is my dynamic compilation course that focuses on virtual-machine design and implementation as well as program analysis. Because of my interest in Web technologies, I emphasize virtual-machines for dynamic scripting languages, such as JavaScript. Students work with Google's V8 JavaScript virtual machine environment and compiler framework for class assignments and projects. Students are intrigued when they realize that the fundamental class of virtual machines extends from managed languages down to binary translators.

My goal in these courses is to empower students with the confidence that in the future they can build these systems on their own and know the trade-offs to make across the hardware and software boundaries.

4 K-12 Outreach: Hands-on Computer Science Using Arduino for 5^{th} and 6^{th} Graders

The promise of a technologically advanced society rests in the hands of the young, and as such, I have a deep interest in developing new academic programs that support STEM education at the K-12 level. My interest is in developing new computer science teaching programs that stimulate the interest of middle and high school students in STEM disciplines by helping them understand how computing impacts lives.

For instance, in conjunction with the UTeach Institute at UT Austin, I designed a series of hands-on inquiry-based lessons that introduce upper elementary students to computer science fundamentals. The course teaches students programming and logic through a unique hands-on and practical approach. We engage the students by having them design projects that affect their lives, and then develop code that animates objects they control by using Arduino-based computers. The lessons have been carefully assessed for effectiveness in a pilot program over summer 2015. Data was collected on the course's effectiveness and attitudinal impact on 50 students, of whom 89% qualify for federal free and reduced meals and 51% are Hispanic. As of fall 2015, the course is being run as a pilot in the Austin Independent School District (AISD). The completed coursework will also supply material to be taught in summer camps at the University. After evaluation and revisions, the lessons will be disseminated through the nationally recognized UTeach

Program at the University of Texas, whose network currently includes 44 universities nationwide. You can find additional details about the program here: https://outreach.uteach.utexas.edu/csp.

I would very much like to continue these sorts of outreach activities in the future at UT. These activities not only benefit the society around me immediately, but they also help in the longer term with my NSF proposals by serving as a platform that helps me disseminate my research findings into the real world.

5 Future Classroom Technology: Wearable Learning for a Better Learning Experience

In addition to developing the existing curriculum and contributing to UT's outreach efforts, I am dedicated to helping UT become a leader in education with the use of next-generation technologies. Over the past decade, much attention has been paid to educating large numbers of students through massively open online courses (MOOCs). In that process, I strongly feel that the needs of the more mainstream traditional classroom environments have been overlooked. Teaching students is becoming challenging because there is a lack of adequate real-time information exchange between the students and the instructor. *I have been exploring how wearable devices can serve as teaching aids to both instructors and students in the classroom, where new educational and assessment strategies need to be developed and technological challenges need to be solved.*

Let us examine a real-world example that demonstrates the scale and complexity of a modern-day classroom at UT Austin for EE319k, which I teach. Fig. 1 shows a large classroom with over 330 students. Such a large classroom environment has long posed a significant challenge in garnering and maintaining students' attention and engaging them in the course material. Even experienced instructors have trouble gathering real-time feedback about the students' engagement. Ideally, such feedback would allow them to dynamically adapt their teaching style and content according to how well students comprehend the material. New teaching styles (e.g., "flipping" the classroom) attempt to address this issue, but even in these situations, engaging with over 100 students simultaneously is very challenging, if not practically infeasible.

Figure 1: A class with over 330 freshman makes real-time interactivity impossible.

Working closely with an undergraduate student and Prof. Christine Julien, I have been prototyping a new wearable-device application that can serve as an effective learning and teaching aid for both students and instructors. Figure 2 shows a student's Google Glass view during lecture in my embedded system's course. Assume that the instructor briefly refers to a previously taught concept, Kirchoff's law. Immediately, the student's smart glass transcribes the keywords in the speech, realizing that the instructor is referring to previously taught content; data-mines the course's website; and displays the relevant slides. The prototype does not have automatic data mining; instead, the course content is manually pretagged, and a search is run on the content when glass's speech recognition software picks up the predefined cues.

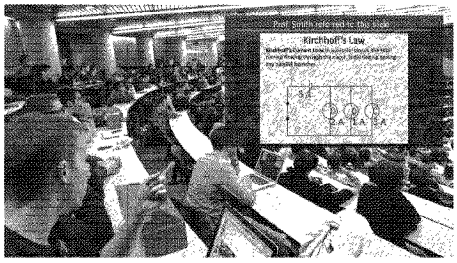


Figure 2: Student's Google Glass view.

The project has numerous education and curriculum development opportunities that I am interested in exploring, such as discovering how to create new lecture material, part of which appears on a student's device while the other part appears on the instructor's projected classroom-wide screen. It also encourages peer-to-peer communication, and possibly a whole new level of social interaction within the class during group activities. It also opens up the need to understand how we assess students differently in the presence of wearable technologies. The project also involves technical challenges that I'd like to study together in conjunction with UT educational innovators, such as developing novel front-end user interfaces and understanding how to provide real-time back-end analytics to enable richer class participation and engagement.

Summary of Teaching

Vijay Janapa Reddi

Table 1. Summary *of Course-Instructor Ratings*

Metric	Value
Total # of students taught in organized courses	229
Average instructor evaluation for UG courses	4.4
Average instructor evaluation for Grad courses	4.3
Average course evaluation for UG courses	4.1
Average course evaluation for Grad courses	4.0

Table 2. Course Schedule by Semester with Number of Students Indicated

Course	F 11	S 12	F 12	S 13	F 13	S 14	F 14	S 15	F 15	S 16
EE319K (Emb. Sys.)						72		54		60
EE382V (CGO)			16		29					
EE382V (Dy. Comp.)		21		8			15			

I was on teaching relief for Fall 2011 and Fall 2015.

[Note: Adjust the number of columns to correspond to the total number of semesters in rank. If the candidate taught less than the normal workload during one or more semesters in rank, provide a brief explanation (i.e. modified instructional duties, buyout of teaching, sick leave).]

Table 3. Summary of Graduate Students *Currently* Supervised at UT Austin

Student *Name*	Co-Supervisor	Degree	Start Date	Date Reached Candidacy	Date Expected to Reach Candidacy	Expected Graduation Date
Yuhao Zhu		PhD	08/2010	03/2016		Fall 2016
Jingwen Leng		PhD	08/2010	03/2016		Fall 2016
Yazhou Zu		PhD	08/2013		Spring 2017	Fall 2018
Matthew Halpern		PhD	08/2013		Spring 2018	Fall 2019
Daniel Richins		PhD	08/2014		Spring 2019	Fall 2020
Wenzhi Cui		PhD	08/2014		Spring 2019	Fall 2020

Vijay Janapa Reddi

Department of ECE

Course Rating Averages

What source was used to complete this chart? My CIS

Course Number: EE319K (Introduction to Embedded Systems)

Semester	Class Size	Number of Responses	Instructor Rating	Course Rating
Fall 2016	68	35	4.3	4.0
Spring 2014	72	37	4.4	4.2
Mean	**70**	**36**	**4.4**	**4.1**

Course Number: EE382V (Code Generation and Optimization)

Semester	Class Size	Number of Responses	Instructor Rating	Course Rating
Fall 2013	29	26	4.4	4.0
Fall 2012	16	13	4.5	4.2
Mean	**23**	**20**	**4.5**	**4.1**

Course Number: EE382V (Dynamic Compilation)

Semester	Class Size	Number of Responses	Instructor Rating	Course Rating
Fall 2014	15	12	4.3	4.1
Spring 2013	8	8	4.4	4.1
Spring 2012	21	19	4.0	3.4
Mean	**15**	**13**	**4.2**	**3.9**

Summary of Recent (All Years In Rank) UT Austin Course-Instructor Survey Resul
Overall Course/Instructor Items

Semester	Course Number	Course Title	Enrollment		Instructor Averages*		College/School Averages**					
			No. of Students Enrolled on 12th Class Day	No. of Surveys Returned at End of Semester	Overall Instructor Rating Avg.	Overall Course Rating Avg.	Overall Instructor Rating Avg.		Overall Course Rating Avg.		No. Classes Surveyed	
Spring 12	E E 382V	DYNAMIC COMPILATION	21	19	4.0	3.4	N/A	***	N/A	***	N/A	
Fall 12	E E 382V	CODE GENERATION & OPTIMIZATION	17	13	4.5	4.2	N/A	***	N/A	***	N/A	
Spring 13	E E 382V	DYNAMIC COMPILATION	8	8	4.4	4.1	N/A	***	N/A	***	N/A	
Fall 13	E E 382V	CODE GENERATION & OPTIMIZATION	29	26	4.4	4.0	N/A	***	N/A	***	N/A	
Spring 14	E E 319K	INTRO TO EMBEDDED SYSTEMS	73	37	4.4	4.2	N/A	***	N/A	***	N/A	
Fall 14	E E 382V	DYNAMIC COMPILATION	15	12	4.3	4.1	N/A	***	N/A	***	N/A	
Spring 16	E E 319K	INTRO TO EMBEDDED SYSTEMS	70	35	4.3	4.0	N/A	***	N/A	***	N/A	

*For the computation of the averages, points were assigned to student responses as follows:
Excellent = 5, Very Good = 4, Satisfactory = 3, Unsatisfactory = 2, Very Unsatisfactory = 1

**College/school averages are the average of class averages, based on all courses surveyed in the instructor's college or school during the academic year in which the course was taught.

***New CIS forms were implemented in the fall 2000 semester. The average rating on the overall course and instructor questions on the new Basic and Expanded forms have been found to be approximately 0.1 to 0.2 points lower than those ratings on the old Common form.

Prepared by the Measurement and Evaluation Center

Peer Teaching Evaluation for ***Prof. Vijay Janapa Reddi***
EE319K Introduction to Embedded Systems

By Andrea Alù (observation date: March 28, 2016, discussion date: April 1, 2016)

April 1, 2016

Summary and Strengths:

The class was held in a large auditorium, and was organized using both a projector and real-time writing and drawing on the board, which was supplemented by working example problems, and questions to students. I unfortunately missed the beginning of the class, as I arrived a few minutes after the start. This was my fault, as I could not find the room in the BUR building.

The lecture was focused on the preparation for an upcoming midterm exam, and focused on several problems, in line with what the exam was expected to focus on. The lecture was well introduced and well prepared, the discussion was clear and linear, the examples were well organized and drew the attention of most of the class. Students were able to follow the pace and were in average quite engaged, probably as much as it can be expected in a lower-level required EE course. Explanations were clear and at a good pace. Questions and comments from students were answered clearly, at a good level and with sufficient length. Prof. Reddi encouraged questions and clearly answered them throughout the class, and the atmosphere was very positive.

Areas for Improvement:

These are all minor issues, to be considered optional.

Writing may be in some instances difficult to follow, especially from the back of the class, where some students may lose attention. This may be improved by using a larger font on the board. In any case, this issue is mostly due to facilities: the large auditorium, with seats relatively far from the projector screen and the blackboard, does not help.

Class involvement may be improved by trying to engage the students sitting in the back. Prof. Reddi gave several opportunities during class to ask questions and comments, and answered very clearly, engaging the class, but the students in the back rows appeared less involved.

The end of class was quite abrupt, it may be used to summarize the discussion and introduce next topics.

Course number and title: EE382N-10: Parallel Computer Architecture

November 30th, 2015

Overall Evaluation: A-

Clarity and effectiveness of presentation:

Vijay gave a guest lecture in my parallel computer architecture class on November 30th on Dynamic Binary Instrumentation of OS Kernel, Driver, and BIOS. He started with an overview of the classic tool, **Pin**, that he helped to develop and moved on to a new tool, Intel SAE, that has significantly more functionality.

Vijay has a lot of passion when he teaches. He is very engaging and animated. He moves around the classroom and uses the boards that are available effectively. It is very clear that he knows the material very well. He understands questions and answers them effectively, providing the right amount of detail. He gave a nice summary at the end of the lecture.

It would have been good to have something to point students to that they could look at right after class. He is describing something new that is not fully available, however, so it is understandable that he could not provide that at this time.

The students are paying attention and engaged.

His speed is a bit too quick on overview material, which probably reduced the number of questions somewhat during that part of the lecture. He got a lot more questions as he slowed down towards the end of the class.

In terms of areas to improve, I would say slow down a bit and ask the class a few more questions during the new material. It might help to slightly reduce the amount of material to be covered.

Overall, the class went very well. I personally learned something very useful today.

Reviewed with Vijay immediately after class.

Derek Chiou
Associate Professor
ECE

Faculty Observed__**Vijay Janapa Reddi**_____ Observed By_____**Lizy John**_____
Date of Observation___**04/17/2014**__ Course Observed___**EE 319K**_____

Comments and Narrative Assessment:

This statement on the teaching of Dr. Vijay Janapa Reddi is prepared by Budget Council Member Professor Lizy John. This statement was prepared following a visit of his class and a review of his course materials.

Dr. Lizy John visited Dr. Janapa Reddi's undergraduate class EE 319K on April 17, 2014. The course is a required lower–division undergraduate course on Embedded Systems Programming taken by all ECE students including EE and CE majors. This is Dr. Reddi's first semester teaching an undergraduate class.

Dr. Janapa Reddi delivered a lecture on embedded systems interfacing and programming, especially on bitmap file format for images. The content was presented clearly. He spoke loudly and clearly. He asked several questions to students and the students responded well. He described the lab assignment and had a demonstration of some relevant lab material. There were about 50 students in the class. They were attentive. Dr. Reddi was able to capture their attention and interest.

Dr. Reddi appeared well-prepared. The visual aids were good. Dr. Reddi used Power Point slides. They were clear and could be easily read from the back of the class. The slides were effective. Dr. Reddi walked around in the class and interacted with the students. Dr. Reddi appeared confident and enthusiastic. He seemed passionate about teaching.

Overall, Dr. Reddi delivered an excellent lecture. I had visited a graduate class of Dr. Reddi in an earlier year. The undergraduate teaching was even better than his graduate teaching. I do not have any concerns on his teaching.

OVERALL EFFECTIVENESS RATING

1 2 3 4 5

4.5

Signature_____ Date___ 04/17/2014

Peer Teaching Evaluation for Vijay Reddi.

I attended Vijay's 382V "Dynamic Compilation" class on April 29th, 2013. Six students attended (I'm not sure about how many students are enrolled, but this is a graduate class.) All seemed excited to be in the class. Vijay gave guidance for the oral final exam that would be given a week or two after. He then covered new topics, which were, in part, extensions and clarifications from throughout the semester.

I was given instructions to evaluate on the following criteria.

1. **Were the students engaged, paying attention?**

Yes, very much so. It was very clear that the students enjoyed being in the class, and were very engaged throughout. Vijay embeds questions into the slides, letting him know when to pause and ask the question. I think that's a very effective way to let the students know when there was a major point and they can think about the question and its answer as Vijay is lecturing on the topic.

There were a lot of questions in addition to those embedded questions. Vijay is very passionate about the subject material and it shows.

2. **Did the professor explain clearly so that the student could get it, or did the professor skip steps or ramble, so it was hard for the student to follow.**

Yes, Vijay explained quite clearly. In a couple of cases, I felt steps were skipped, but it was clear from the questions that those steps had been discussed in the past.

3. **Was the pace of the lecture right.**

Yes. The pace was fast, and very fast during an introduction to a topic, but it was clear that the introduction was simply a summary of what had been covered before. Once he got to the new material he was still fast, but the questions coming from the students clearly indicated that the pace was fine for them. I think had the class had weaker students, it would be too fast, but I think for this particular set of students, it was fine. I know many of the students in his class, who are some of the very best students in our department.

4. **Did the professor provide appropriate context for the material so the student could see where it fits into the larger scheme of things.**

Yes. Before every new topic, a summary of the previously covered material is given. Vijay sometimes jumps around, but the students were keeping up.

Additional comments

Vijay's teaching methods were very effective and appropriate for this class. He may be too fast for a weaker class, but I think he had tuned his pace for this particular set of students.

There was a lot of material covered, probably too much if it was a normal lecture, but this was partially a review for the oral exam.

Some of the text on the slides could be a bigger.

Derek Chiou

Faculty Observed__**Vijay Janapa Reddi**_____ Observed By_____**Lizy John**_____
Date of Observation___**04/30/2012**__ Course Observed___**EE 382V**_____

Comments and Narrative Assessment:

This statement on the teaching of Dr. Vijay Janapa Reddi is prepared by Budget Council Member Professor Lizy John. This statement was prepared following a visit of his class and a review of his course materials.

Dr. Lizy John visited Dr. Janapa Reddi's graduate class EE 382V on April 30, 2012. The course was entitled Dynamic Compilation. The course is a specialized graduate course focusing on a very specialized modern aspect of code compilation. The course is related to Dr. Reddi's research area and is developed by Dr. Reddi himself. This is Dr. Reddi's first semester teaching.

There were about 20 students in the class. They were attentive. Dr. Reddi was able to capture their attention and interest.

Dr. Janapa Reddi delivered a lecture on Reliability Wall and explained how hardware software co-design is important. The content of the lecture was clear to the students. Relevancy of the main ideas was clear in the presentation. Students interacted with the instructor during the lecture. Out of the 20 students in the class, more than 10 asked questions. Many asked multiple questions.

The visual aids were good. Dr. Reddi used Power Point slides. They were clear and could be easily read from the back of the class. The slides were effective. Dr. Reddi appeared confident and enthusiastic.

Overall, Dr. Reddi delivered a good lecture. But it would be worthwhile to visit an undergraduate class taught by Dr. Reddi in the future, so one could evaluate his teaching ability for more basic material.

OVERALL EFFECTIVENESS RATING

1 2 3 4 5

4

Signature_____ Date___ 04/30/2012

NAME	EID	LAST SEM	COMM POSITION	MAST OR DOCT	DEGREE	FIELD	YYS	2ND DEGREE	FIELD	YYS
CHAUHAN, HIMANSHU	hc8445	169	MEMBER	D						
GARG, ANKITA	ag35278	132	CO-CHAIR	M	M.S.COMP.SC	COMPUTER SCIE	20132			
HALPERN, MATTHEW FRANKLIN	mh33338	169	CHAIR	M	M.S.E.	ELECTRICAL AN	20162			
JO, JUNGHO	jj3354	159	MEMBER	D						
KALEEM, RASHID	rk6954	169	MEMBER	D						
KIM, DONG WAN	dk9744	169	MEMBER	D						
KIM, YOUNGTAEK	yk3582	132	MEMBER	D	PH.D.	ELECTRICAL AN	20132			
LEE, IKHWAN	i12452	156	MEMBER	D	PH.D.	ELECTRICAL AN	20156			
LENG, JINGWEN	j142849	169	CHAIR	D						
RAZAGHI, PARISA	pr6689	142	MEMBER	D	PH.D.	ELECTRICAL AN	20142			
REED, DOUGLAS RAYE	drr348	152	CHAIR	M	M.S.E.	ELECTRICAL AN	20152			
RHU, MINSOO	mr35987	142	MEMBER	D	PH.D.	ELECTRICAL AN	20142			
SRIKANTH, ADITYA	as53435	132	CHAIR	M	M.S.E.	ELECTRICAL AN	20132			
YUAN, YI	yy2833	169	MEMBER	D						
ZHU, YUHAO	yz4422	169	CHAIR	D						

List of Postdoctoral Fellows Supervised

Vijay Janapa Reddi

No postdoctoral fellows supervised.

Budget Council Assessment on Research for Faculty Promotion Candidate Dr. Vijay Janapa Reddi

This statement on the research of Assistant Professor Dr. Vijay Janapa Reddi was prepared by Budget Council Member Professor Lizy K. John (with assistance from Associate Professor Mattan Erez). This statement was prepared following a review of his vita, his research papers, his external letters, and knowledge of his research.

Dr. Vijay Janapa Reddi's research is on computer architecture, focusing on the hardware software interface, and cross-layer optimizations to improve the performance, energy consumption, and reliability of computing platforms ranging from mobile computers to data centers. His research involves co-design of various hardware and software layers to eliminate performance and energy inefficiencies. He bridges the gap between hardware and software, focusing on determining architectural mechanisms and programming abstractions for improving performance and propagating efficiency throughout? the computer system.

This fundamental cross-layer approach is evident in all of Dr. Janapa Reddi's research. The cross-layer work also often necessitates diving into commercial software and hardware and developing new methodologies and tools. Conducting this type of research is extremely challenging, and few in the computer architecture community choose to pursue the cross-layer approach in full. Dr. Janapa Reddi does not shy away from this challenging task. In fact, he relishes it and is conducting such research on mobile web platforms, many-core accelerators for heavy compute tasks, and architectures for cloud systems. The tools and techniques Dr. Janapa Reddi is developing as part of this research are significant contributions, on their own, and they are an important and unique aspect of his research. The paragraphs below discuss his intellectual and methodological contributions.

Dr. Janapa Reddi's research has made significant contributions in the **energy-efficiency of mobile computing**. He has architected a processor core for efficient mobile web browsing called Web-core. (Most users now turn to their cell phone before their computer, if they even have one.) (or: Many people use their cell phones for tasks that they once performed on their computers.) The most common tasks performed revolve around accessing information from the web, rendering that information, and interacting with the user. The mobile web browser encompasses all these actions, and is typically the most used interactive application on a mobile device. At the same time, the mobile browser is a very complex and demanding application that is poorly understood by computer architects. From the computer architecture perspective, Dr. Janapa Reddi is one of the pioneers in researching mobile platforms and browser application. His research not only resulted in the Web-core architecture, but has also led to new metrics and evaluation methodologies, as well as the new GreenWeb abstractions and software interfaces. Dr. Janapa Reddi also extended this work into the browser and web-application software layers and proposed web interfaces and language extensions that take advantage of the new insights, techniques, and mechanisms he pioneered. For example, a new event-based scheduling scheme for mobile web browsers that he has architected is being evaluated for integration into Samsung's Tizen Operating System.

Dr. Janapa Reddi's second line of research, while a member of our faculty, is on many-core processors. Specifically, Vijay has made significant contributions to **improving energy efficiency by reducing voltage guardbands on many-core CPUs and GPUs**. Dr. Janapa Reddi demonstrated how voltage noise in many-core and heterogeneous systems differs from prior (mostly) single core work. His effort laid the groundwork for guardband optimizations in GPUs. He developed open-source simulation frameworks (GPUVolt, GPUWattch) and used measurements to show new insights on how the integration between CPU and GPU platforms can lead to new voltage noise challenges. By applying a cross-layer approach, this work demonstrated the significant energy reduction potential with existing commercial platforms.

As an Assistant Professor, Vijay's research has also led to his design of innovative cross-layer solutions across languages, operating systems, and architecture to create **efficient scheduling techniques and processors for cloud-based applications**. Dr. Janapa Reddi observed that many cloud-based applications utilize an event-driven execution model in both the user device and cloud components. Dr. Janapa Reddi analyzed such software, which exists in real systems but for which standard research benchmarks do not exist. Again, applying a cross-layer approach he is researching a new processor architecture specifically for these event-driven execution models and workloads.

As mentioned earlier, an important and impressive aspect of Dr. Janapa Reddi's research is that it embraces the most challenging and difficult aspects of computer architecture research: working with real systems, researching real applications that do not have existing standard benchmark suites, and that require **new analytic tools and techniques**. The fruit of this research goes way beyond the direct intellectual contributions of the research. The new benchmarks, metrics, and tools developed have provided a way for other researchers to enter the fields Dr. Janapa Reddi pioneered.

This aspect of Vijay's research started before he joined our faculty. While at Intel, he helped create the "Runtime Systems for Program Introspection, Optimization, and Analysis," better known as the **Pin binary instrumentation engine**. Pin is one of the most-widely used tools in the computer architecture research and programming and software systems communities. Pin has enabled an active research community that created diverse tools for architecture exploration, workload analysis, program security, and application emulation. Since 2003, Pin has over 2,500 citations and close to 150,000 downloads.

While on our faculty, Dr. Janapa Reddi has continued developing and releasing new tools that are both required for his research and are broadly used by the community. One example is his effort to remedy some of the shortcomings of Pin. Despite its proven usefulness, Pin is limited in that it can only analyze programs, rather than an entire system. The **Simulation and Analysis Engine (SAE)** he has recently co-developed fixes this problem by bringing the usability and universality benefits of Pin-like instrumentation to system components in addition to the program itself. This enables the analysis of emerging big data and other scale-out workloads. There is no reason to doubt that this tool will likely usher in promising new research insights, as Pin did, with the emergence of Big Data workloads.

The tools above provided a major boost to the architecture research community. Yet, Dr. Janapa Reddi's efforts in developing new tools and methodologies don't stop there. To enable his research on many-core processors, he created the **GPUWattch and GPUVolt modeling tools**. GPUWattch models the power consumption of various components in a many-core accelerator based on a graphics processing unit and

has been validated against real hardware. Power is a major concern for computer architects, and GPUWattch has already been cited 199 times since its publication in 2013. GPUVolt integrates with GPUWattch to simulate the voltage distribution across time and space in a GPU. This tool has enabled an unprecedented level of rigor when researching methods to improve power efficiency by reducing guardbands. As with the other tools and models, Dr. Janapa Reddi validated the predictiveness and accuracy of GPUVolt with the behavior of real hardware. Dr. Janapa Reddi is the first, and only, researcher in our field who is tackling the challenging problem of studying mobile devices and browsers. In this research, Dr. Janapa Reddi introduced new modeling techniques, new workloads, and new metrics that incorporate user experience and not just traditional performance and power metrics.

Dr. Janapa Reddi's publication record is extremely strong. His research has resulted in 34 conference papers (20 since joining UT). All of these conferences are peer-reviewed conferences with archived proceedings. He has also published 8 journal papers (3 in rank). In the computer architecture area, conference papers in the top-tier conferences are considered superior to journal papers. His publications include 3 papers in the field's flagship conference ACM/IEEE International Symposium on Computer Architecture (ISCA), 3 in IEEE/ACM International Symposium on Microarchitecture (MICRO), 5 in IEEE High Performance Computer Architecture Symposium (HPCA), and 2 in ACM Conference on Programming Language Design and Implementation (PLDI). The acceptance rates for the ISCA conference in the years he published have been 18%, 19% and 18%, whereas the MICRO conference had acceptance rates of 20%, 22%, and 25%. The acceptance rates for his PLDI papers have been 16% and 21%, while the acceptance rates for the HPCA papers ranged from 19% to 23%. His H-index on Google Scholar is 20, and the h-index since 2011 is 17, which are impressive numbers considering the early stage of his career.

Dr. Janapa Reddi's work has been rewarded with several best paper awards. In 2015, he won the ACM Special Interest Group on Programming Languages (SIGPLAN) Most Influential Paper Award to recognize the impact his 2005 PLDI paper has had on the field. He also won the best paper award at IEEE/ACM International Symposium on Microarchitecture (MICRO) 2005, where one award was given from the 29 accepted papers out of 147 submissions. Additionally, his paper also won the best paper award at the IEEE High Performance Computer Architecture Symposium (HPCA) 2009 where one paper was selected out of the 34 accepted papers from 184 submissions. In addition, his papers were selected three times in the IEEE/ACM International Symposium on Microarchitecture (MICRO) Top Picks, where the IEEE MICRO magazine selects 10-12 of the year's best research papers from 5+ top computer architecture conferences based on novelty and potential long-term impact. This is truly exceptional considering that he is still in the early stages of his career.

Dr. Janapa Reddi has served as PI or co-PI on 7 successful grant proposals, with his share totaling to $1.127 million in contracts and an additional $684 K in research gifts. The industry gift amount is significant and indicates how much the industry values Dr. Janapa Reddi's research. First and foremost, Dr. Janapa Reddi has received four NSF grants for his research on energy efficient and reliable computing. This includes a sole-PI grant for $400K for mobile web computing. Another supporter of his research is the Semiconductor Research Consortium (SRC), which is supporting Dr. Janapa Reddi's research on resilient near-threshold systems. Dr. Janapa Reddi is integrating concepts of energy efficiency and reliability.

Dr. Janapa Reddi's research is regarded highly by the community, as evidenced by the recent awarding of the prestigious IEEE Technical Committee on Computer Architecture (TCCA) Young Computer Architect Award, 2016. This award is given annually to a young computer architect within 6 years of his/her PhD. Dr. Janapa Reddi received the award "in recognition of his outstanding research contributions in mobile computing and resilient architectures." A member of the committee remarked that Dr. Janapa Reddi stood out from the many promising young computer architects by a significant margin. The award also testifies that he is the top computer architect among his peers.

The external reviewers emphasized the quality and relevance of Dr. Janapa Reddi's research. Consider the following excerpts from the external reviewer letters:

Dr. Chita Das, Penn State (IEEE Fellow):
"Vijay is internationally known for his accomplishments in the broad area of computer architecture."

"Vijay is a pioneer in the area of designing energy-efficient mobile architectures."

Dr. Josep Torrellas, Illinois (IEEE and ACM Fellow):
"Prof. Reddi's work is influential. It is being followed by other researchers …."

"People in companies are certainly listening to his work."

Dr. Matt Welsh, Google (Lead of Chrome Cloud team, former Harvard professor):
"He is one of the few researchers -- indeed, **the only researcher to my knowledge**, -- bringing both architecture and OS ideas to bear on this set of problems [energy efficiency of the web].

"Vijay's work is right in the bullseye of the set of problems we care about."

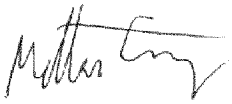
"an exceptionally strong track record that spans the architecture, programming language, operating systems, and mobile research communities. His work is creative, impactful, cross--disciplinary, and hugely relevant to important challenges"

Dr. Scott Mahlke, Michigan:
"Prof. Reddi is an outstanding researcher and respected scholar..."

"Prof. Reddi has already had a profound impact creating tools that are seamlessly used by students, faculty, engineers…."

In summary, Dr. Vijay Janapa Reddi has developed a great research foundation for the future, with a good set of students and a well-funded research lab. His papers have been well-cited for a researcher at his stage of career. He seems well-positioned to continuing his success. Vijay has a track record of strong commitment to not only conduct cutting-edge research, but also enable others to do novel research as well.

Summary prepared by:
Budget Council Member Professor Lizy Kurian John and Associate Professor Mattan Erez.



Five Most Significant Publications (in Rank)
Prof. Vijay Janapa Reddi

Dept. of Electrical and Computer Engineering,
The University of Texas at Austin,
vj@ece.utexas.edu

1. S. Campanoni, T. Jones, G. Holloway, **V. Janapa Reddi**, G. Wei, D. Brooks. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing." in IEEE/ACM International Symposium on Code Generation and Optimization (CGO), pp.84-93, March, 2012. http://dx.doi.org/10.1145/2259016.2259028

2. Y. Zhu, **V. Janapa Reddi**. "High-Performance and Energy-Efficient Mobile Web Browsing on Big/Little Systems," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.13-24, February 2013. http://dx.doi.org/10.1109/hpca.2013.6522303

3. J. Leng, T. Hetherington, A. ElTantawy, S. Gilani, N. Kim, T. Aamodt, **V. Janapa Reddi**. "GPUWattch: Enabling Energy Optimizations in GPGPUs," in ACM/IEEE International Symposium on Computer Architecture (ISCA), vol 41(3), pp.487-498, June 2013. http://dx.doi.org/10.1145/2485922.2485964

4. Y. Zhu, **V. Janapa Reddi**. "WebCore: Architectural Support for Interactive Mobile Web Browsing," in ACM/IEEE International Symposium on Computer Architecture (ISCA), pp.541-552, June 2014. http://dx.doi.org/10.1109/isca.2014.6853239

5. J. Leng, Y. Zu, V. **Janapa Reddi**. "GPU Voltage Noise: Characterization and Hierarchical Smoothing of Spatial and Temporal Voltage Noise Interference in GPU Architectures," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.161-173, February 2015. http://dx.doi.org/10.1109/hpca.2015.7056030

Research Statement

Vijay Janapa Reddi

1 Overview

I am a computer scientist by training who bridges hardware and software to solve important problems in systems. Over recent years, the landscape of computing has largely bifurcated into two extreme domains: mobile and datacenter-centric computing. I have expertise in both of these domains, where achieving performance improvements, managing power, and building reliable systems has become increasingly hard.

My approach involves the co-design of architecture, compilers, and application software to eliminate performance inefficiencies at the circuit, (micro)architecture, and system level that impact energy efficiency and reliability. Looking ahead, I believe that vertical co-design across the system stack is necessary because generational improvements in processor and system performance have largely plateaued, and it has become increasingly difficult to build reliable systems in the face of deep nanotechnology scaling challenges.

In this statement, I summarize my key contributions and ongoing effort in both of the computing domains. In **mobile computing** (§ 2), I focus on exploiting the trade-offs between user experience, power management, and processor capabilities for an extremely important application domain — the mobile Web. In **datacenter computing** (§ 3), I focus on energy-efficient and resilient Exascale computing by harnessing the unique capabilities of heterogeneous computing resources, including asymmetric CPU architectures and GPUs. Finally, I lay out my research plans and ambitions for the next five to seven years (§ 4).

2 High-Performance, Energy-Efficient Mobile Web Computing

Mobile computing is here and will dominate the future. A key observation about mobile computing is its intertwined relationship with the Web. The Web is continuously transforming society—shaping communications, catalyzing innovations, and even shaping thought processes. Over the past decade, the role of the Web has shifted from information retrieval (Web 1.0) to providing a platform for interactive and engaging user experiences (Web 2.0). The Web is once again entering a new age, transcending user engagement to provide intelligent services that can seamlessly integrate multiple types of devices (i.e., the Web of Things).

My work is concentrated on the relationship between mobile devices and Web technologies. The proliferation of the Web rests largely on the hardware's capabilities. Mobile devices struggle to deliver high computational capability on a battery-energy budget that meet applications' computing and users' quality-of-experience (QoE) requirements. Moreover, each device generation is expected to compute faster, last longer and accommodate more peripherals into thinner form factors. I show that the mobile CPU's rise to power has staggering energy and thermal implications on future mobile system designs [1], and that bridging the gap between computing capability and the software stack is crucial going forward [2].

The solutions I developed with my students establish the foundations needed to develop future high-performance and energy-efficient mobile computing systems that can usher in the next-generation Web. The value of the research is based on the involvement of synergistic cross-layer optimizations across the hardware, software, and application layers to maximize system efficiency. I take a holistic view of the mobile Web, spanning mobile applications, Web (browser) runtime, and the underlying processor architecture.

Web Language Extensions: Mobile application designers ideally need to optimize for energy efficiency while satisfying the end-user QoE. However, the traditional interface between Web applications and the browser, i.e., the Web languages (HTML, CSS, and JavaScript), is purely task or functionality centric and contains little QoE information. I believe that the conventional Web languages should be extended so that application developers explicitly express application QoE characteristics and user QoE requirements.

My group pioneered GreenWeb, a system that describes and implements the concept of extending existing Web languages (HTML, CSS and JavaScript) with a set of pragma and annotation APIs for developers to express application QoE characteristics [3]. Given the language "hints," the underlying system can better perform optimizations such as trading off performance for energy consumption without sacrificing user

QoE. GreenWeb shows significant energy savings (21.2% to 67.5%) over Android's default Interactive governor that is designed for power saving, and it has few QoE violations on state-of-the-art smartphones.

Web-Specific Processor Architecture: Generational improvements in processor energy-efficiency cannot continue to be derived from making transistors smaller because transistor scaling and voltage scaling are no longer in line with each other. Thus, processor power densities can far exceed tolerable design points, and, therefore, a large portion of the silicon must remain "dark." Simply instantiating more cores, as the industry has been doing, will not help us achieve energy efficiency, and it is not sustainable.

However, I believe we can achieve energy efficiency with *domain-specific hardware specialization*. The challenge is in understanding how to balance specialization with general-purpose programmability in the mobile Web context. Web technologies rely on general-purpose programmability because they are large and complex pieces of software, often written using a combination of different programming languages. For example, the Google Chrome Web browser is written in 29 different languages.

My group designed the WebCore [4], a synthesizeable general-purpose core that's specialized for mobile Web applications and balances specialization with programmability. It executes mobile Web applications with extreme efficiency because its microarchitectural structures are tuned for frequently executed Web computational tasks, and it is augmented with hardware accelerators for kernels found in the HTML rendering engine, CSS kernels, etc. To save power, WebCore becomes "dark" when there are no Web tasks to execute. I envision that WebCore will become a standard processing core in every future multicore system-on-chip (SoC) device. The WebCore can be easily integrated into SoCs by leveraging standard bus protocols that connect on-chip IP, custom logic, and specialized functions in a generalized plug-and-play manner.

Web (Browser) Runtime: If current mobile evolution trends continue, new mobile Web applications will emerge rapidly, and the architecture will evolve continuously. Mobile Web applications will have richer semantics, such as GreenWeb's QoE information, and the architecture will embrace domain-specific processor architectures, such as the WebCore, to provide better runtime optimization opportunities to software. But applications and the architecture have always required good runtime support to run efficiently.

To glue applications that are annotated with QoE information with architectures that are increasingly more sophisticated, my group enhanced Web browsers with smarts to enable feedback-directed optimizations. We created components that extended Web browser engines (Firefox and Chrome) so that the new Web language extensions connect with the WebCore [4, 5]. We also created new components within the browser to make predictions about how best to execute a given web application in- put on the hardware [6, 7]. The enhanced browser runtime dynamically matches hardware resources with application characteristics and user requirements to minimize energy consumption while meeting user QoE expectations. We demonstrated a working prototype using the Google Chromium and V8 framework on a Samsung Exynos 5410 SoC (used in the Galaxy S4 smartphone). Based on real hardware and software measurements, we achieved a 55% energy saving with only 0.4% of QoE violations that were perceptible to end users.

Impact: My work has real-world impact, a tenet I deeply value as a researcher. Over 1.5 billion users rely on the mobile Web computing stack on a daily basis for information retrieval and processing. It is not often that a computer architect can say that the effort in a single application domain can affect the lives of a billion people with an instantaneous push. The "products" of my research have resulted in numerous industry engagements for practical deployment, Google for the language support and software algorithms and Samsung for the hardware innovation. We have discussed how the language extensions would affect developer productivity, as well as result in abuse of the hints that can have a detrimental impact on performance or power. Samsung is evaluating the EBS scheduler [5] in their Tizen operating system, which is a fully web-based operating system. There is significant room for further innovation because the Web is still emerging as the "ambient" application development platform (i.e., the new managed runtime).

3 Energy-Efficient Datacenters and Reliable Exascale Systems

On the other extreme of mobile computing, power is also a major challenge for both mainstream commercial datacenters and supercomputers that support society and the nation's scientific advancements, respectively. My work pursues innovative application-specific solutions that are a significant departure from most main-

stream efforts. On the CPU side, I helped introduce and evaluate the radical idea that datacenters use small, power-efficient mobile processors instead of big, power-hungry server processors. On the GPU side, as well as CPU side, I have shown how carefully relaxing the margins that are built in for reliability, both with hardware and software assistance, can offer large efficiency improvements for exascale systems.

3.1 Low-Power Mobile Processors for Datacenters

One of the biggest and ongoing contentious debates in the industry is whether we should abandon high-performance, out-of-order, superscalar, speculative processors and revert to simpler in-order processors that are more power efficient. Smaller and simpler cores in numbers offer task-level parallelism in exchange for higher per-task latency. Whether or not we can make this smooth transition from big cores to small cores is of extreme importance to warehouse-scale computers, as well as extremely large datacenters.

Wimpy Cores: I proposed "Web Search Using Small Cores." [8, 9]. Together with researchers at Microsoft, I spearheaded an in-depth evaluation of running Microsoft's Bing search engine, a next-generation machine learning-based datacenter workload, on low-power mobile processors. We found that mobile processors offer a 5x performance-per-Watt efficiency improvement for emerging workloads over traditional server processors. However, mobile processors can detrimentally impact application quality-of-service robustness and flexibility. These challenges constitute the "price of efficiency." Our results warn us that the transition from big to small cores might not be smooth. For instance, tail latencies worsen significantly.

My group is in the process of rearchitecting small cores to efficiently support emerging datacenter workloads. Several questions arise, such as whether we are bound to using at least some big cores along with small cores, or whether there are optimization opportunities at the small(er) core level alone. We completed a comprehensive characterization of mobile CPU capabilities and projected their growth into the future to identify the critical challenges [1]. From an architectural perspective, the study reveals that one possibility is to combine small cores with accelerators. Accelerators dominate mobile SoC processor designs. General-purpose mobile CPUs occupy only about 16% of the entire SoC die area, and the rest is almost exclusively dedicated to specialized application-specific task accelerators. Thus, we are in the process of determining how small cores coupled with new SoC accelerators can improve datacenter energy efficiency.

Event-driven Processors: In my group's analysis of emerging cloud workloads [10], we discovered a much-needed critical application insight to empower small cores. Emerging workloads are increasingly being built around the event-driven programming model paradigm. Events are loosely defined as external user inputs or internally generated computation tasks. Individual events can comprise millions to billions of instructions. They can also trigger other events. Events, as they occur, are sequentially enqueued and then dispatched one after the other in a restricted first-in, first-out manner to the processor for execution. These events can sometimes be independent of one another; there is typically little inter-event communication, and they can execute in parallel on the low-power, small cores to achieve energy efficiency.

We are currently designing Eve—a spatial, event-driven processor architecture—to exploit parallelism and locality characteristics unique to event-driven execution. In Eve, an event-driven application begins execution on the general-purpose cores, dynamically offloading events to a customized sea of low-power, highly efficient small event cores for execution. Event offloading is performed transparently without modification to the native application. A compiler performs the task partitioning between the CPU and the event processors while a runtime system monitors event-execution and optimizes execution on-the-fly.

Impact: The seeds of the wimpy core research can be found in the real world in companies such as SeaMicro, HP, Intel and others, which in recent years adopted low-power x86 processors for high-density microservers. The research from the work has also been highly sought after by software and hardware companies, including Google, Facebook, Samsung and Qualcomm, which are building their own hardware. In academia, the research sparked new work at Stanford involving mobile memory use in server platforms.

3.2 Software-Assisted, Hardware-Guaranteed Resiliency for Exascale Systems

During the past decade, system designers have aggressively sought efficient design points on power, performance, and cost. Of these, power has emerged as a first-order design challenge for future Exascale

systems. Unfortunately, operating a system close to a peak efficiency design point for power can make the system susceptible to unreliability, whereas preallocating large margins or guardbands makes the system inefficient. The interplay between reliability, power, and performance has largely remained under explored. I focus on understanding this interplay and co-designing the hardware and software layers to build high-end, energy-efficient CPU and GPU systems that specifically benefit supercomputing systems.

I investigated several techniques to build computing systems that achieve high energy efficiency without compromising reliability. They are centered around a resilient *software-assisted, hardware-guaranteed* machine organization [11] in which a runtime continuously monitors execution and adapts hardware configuration based on feedback. The system relies on hardware for an immediate reaction (albeit suboptimally) to reliability "emergencies," such as transient power and voltage fluctuations. The system utilizes software's global knowledge of activities across the platform to eliminate repeated occurrences of such hardware emergencies. The co-design results in a resilient system without compromising energy efficiency.

Many-Core GPUs: My research group pioneered the work in understanding how to relax guardbands in GPU systems for energy efficiency without compromising performance and reliability. We showed that on commercially available off-the-shelf GPU hardware there is a 20% voltage guardband, which, if "eliminated" completely, can result in up to 25% energy savings [12]. We also quantified how the exact improvement magnitude depends on the program's available guardband using real chip measurements [13]. We performed detailed simulations [12], using new tools we built that are now open sourced and widely used by other researchers [14, 15, 16], to make fundamental observations about the program- and kernel-dependent V_{min} behavior needed to perform V_{min} reduction optimizations. We discovered machine learning methods to predict the program and kernel V_{min} accurately on-the-fly [13]. Our research opens up new possibilities for a cross-layer dynamic guardbanding scheme on GPUs, in which software predicts and manages the voltage guardband while correctness is ensured by a hardware fail-stop mechanism.

Multicore CPUs: We have also made seminal contributions in how to relax guardbands in CPUs. We built the first hardware voltage emergency predictor to predict emergencies in due time to take preventive action [17]. A key outcome of the predictor work is in, for the first time, showing that recurring program and microarchitectural activity combined with the interactions of the underlying power delivery subsystem repeatedly cause emergencies [18, 19]. The discovery enables alternative (non-)predictor solutions to mitigate emergencies. At the software level, we pioneered and developed the concept of "voltage smoothing", i.e., the process of eliminating emergencies altogether either by transforming program code on-the-fly [20, 21] or scheduling collaborative program threads carefully together on a multicore processor using operating system assistance [22]. With the advent of adaptive timing guardband management, we show, yet again for the first time, that adaptive guardbanding turns the processor's power delivery subsystem into a shared resource [23, 22], and that sharing power delivery in multicore poses a fundamental constraint on adaptive guardbanding's behavior. Using a POWER7+ multicore processor, one of the few commercial systems that offers adaptive guardbanding today, we show that a cross-stack approach, involving the architecture and operating system, can mitigate the multicore scaling inefficiency we discovered in real systems [24].

Impact: My research resulted in companies, such as IBM, Intel and AMD, actively seeking out research collaborations with my group. Moreover, we are currently collaborating with Pacific Northwest National Laboratory (PNNL) to develop an Exascale runtime for resiliency to evaluate several aspects of the work for a supercomputing system. Also, the work has received wide recognition over the years, including being chosen as the Best Paper at MICRO'05 and HPCA'09 and selected for the IEEE Micro Top Picks in 2009 and 2010. I have also written invited keynote articles [25, 26] on the topic, served as an invited guest editor for an IEEE Micro special issue on reliability-aware design [27], and written a Synthesis Lecture manuscript [28].

4 Future Research Directions

I will *continue* establishing energy saving mechanisms within the mobile Web (§ 2), build high-performance mobile systems (§ 3.1), and architect resilient systems through hardware and software co-design (§ 3.2). However, I *also* want to revitalize (1) compilation, (2) runtime environments and (3) architecture research by leveraging the unique opportunities offered by an increasingly connected mobile ecosystem as follows:

(1) Web Crowdsourcing Compiler: Traditional compilers and runtime systems suffer greatly from *local*, device-specific program scope. Instead, we are developing the Web Crowdsourcing Compiler (WebCC). WebCC leverages the global crowdsourcing power (i.e., obtaining information from a large group of devices) to mitigate runtime bottlenecks. WebCC exploits *"user-level parallelism"* to forward a mobile application's runtime profile information from one device to another to mitigate system overheads. By collecting runtime profile information in the cloud, gathered from an application's execution on one or more mobile devices, with one or more users, WebCC improves mobile performance and reduces energy consumption.

(2) Cognitive Cyberphysical Runtimes: There will be over 50 billion web-enabled edge devices by 2020. Managing these users and devices under various power, performance and reliability constraints will prove challenging, if not impossible if we rely on existing current application development and device management solutions. I envision building a new, thin WebOS—a platform on top of which we can evaluate several research challenges, as I believe that Web technologies are the key to the success of cyberphysical computing. My research group has unique expertise and in-depth knowledge of Web technologies. Taking the Web's fundamental characteristics and baking them into an OS-like environment would offer numerous benefits. First, the Web is inarguably the single most unifying platform across the world; where connectivity matters, the Web wins. Second, Web technologies are mature, and they offer many of the key components that are required for device operation, management, etc., and are inherently resilient. Third, devices can be seamlessly programmed in high-level managed languages, while abstracting away hardware idiosyncrasies, of which there are often many due to severe hardware heterogeneity in the cyberphysical world.

(3) Machine Learning Architectures for Big Data Systems: Machine learning based big data science has the potential to unlock new discoveries. However, the challenge lies in sifting through petabytes of data to find the "needle in the haystack." Data scientists often use commodity hardware and rely on scripting language frameworks, such as Lua, Python and Scala, for processing big datasets as these frameworks often come with prepackaged computational algorithms and machine learning libraries for mining big datasets. There is a need for new architectures that are specifically optimized for these types of frameworks.

I want to develop new co-processing architectures for machine learning that can enable high-performance processing for enabling rapid big data science discoveries. Scripting languages are dynamically interpreted languages based on managed runtimes that could benefit from hardware support for such tasks as garbage collection, graph traversals, etc. So I wish to identify the bottlenecks in these managed runtimes when they are processing big datasets, seek out opportunities for hardware acceleration of the computational algorithms (possibly using FPGAs) and investigate hardware-software co-design optimizations.

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Vijay Janapa Reddi

Table 1. Research Summary

Metric	Value
Peer-reviewed journal publications (in rank ***and total***)	4 / 9
Peer-reviewed conference proceedings (in rank ***and total***)	19 / 33
Number of ***journal*** papers ***in rank*** with UT students ***as co-authors***	2
Total citations of all publications (career) ***from ISI Web of Knowledge***	333
h-index (career) ***from ISI Web of Knowledge****	7
Total citations of all publications (career) ***from Google Scholar or Publish or Perish***	4220
h-index (career) ***from Google Scholar or Publish or Perish****	19
Total external research funding raised	$2,403,959
Total external research funding raised (candidate's share)	$1,810,670
Total number of external grants/contracts ***awarded***	7
Number of external grants/contracts ***awarded*** as PI	5

Note:

* ***Provide a printout/screen shot of the first page of the report from both ISI Web of Knowledge and Google Scholar***

Table 2. External Grants and Contracts Awarded while in Rank

Grants and Contracts

PI/Co-PI	Title	Agency	Grant Period	Total/ My Share
PI Janapa Reddi (self)	High-Performance, Energy-Efficient Mobile Web Computing	National Science Foundation	06/01/2016 - 05/31/2019	$400,000/ $400,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Second Phase of Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	04/10/2015 - 01/10/2016	$100,000/ $43,500
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-Driven Resiliency for Near-Threshold Systems: under SRC MAG (201300745-001;2013-HJ-2408 MAG)	Semiconductor Research Corporation	04/01/2013 - 03/31/2017	$128,000/ $64,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	12/15/2013 - 01/15/2015	$100,000/ $43,500

PI Janapa Reddi/ Co-PI Sek Chai (SRI)	Resilient Computing Systems Using Deep Learning Techniques	National Science Foundation	08/01/2015 - 07/31/2018	$499,959/ $265,000
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-driven resiliency for Near Threshold Systems	National Science Foundation	04/01/2013 - 03/31/2016	$192,000/ $96,000
PI Janapa Reddi/ Co-PI Lizy John (UT Austin)	Cross-Layer Solutions for Sustainable and Reliable Computing Solutions	National Science Foundation	08/01/2012 - 07/31/2015	$300,000/ $214,670

Industry Gifts

PI/Co-PI	**Title**	**Agency**	**Grant Period**	**Grant Total**
PI Janapa Reddi (self)	Mobile computing	Google	2012, 2013, 2015	$139,000
PI Janapa Reddi (self)	Reliability and Mobile Computing	Intel	2012, 2013, 2015, 2016	$395,000
PI Janapa Reddi (self)	Power modeling	AMD	2012, 2013, 2014, 2015	$150,000

Total Funding: **$2,403,959**

My Total Funding: **$1,810,670**

Note:

† For all projects, list the role of the candidate. For projects with co-investigators, also list name, role (PI or Co-PI), and department (university if not UT) for each co-investigator.

Division of Labor – Research Projects

Vijay Janapa Reddi

The division of labor for research projects/grants while in rank is provided in the table below. Only collaborative projects are listed. The complete list of all awarded grants is present in my CV.

Grants and Contracts

PI/Co-PI	Title	Agency	Division of Labor	Total/ My Share
PI Janapa Reddi (self)	High-Performance, Energy-Efficient Mobile Web Computing	National Science Foundation	VJ: 100%	$400,000/ $400,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Second Phase of Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	CK: 50% VJ: 50% (I was responsible for the architecture piece of the work, while Chris was responsible for the circuits part)	$100,000/ $43,500
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-Driven Resiliency for Near-Threshold Systems: under SRC MAG (201300745-001;2013-HJ-2408 MAG)	Semiconductor Research Corporation	VJ: 50% CK: 50% (the project was on circuit and architecture co-design. I was responsible for the architecture half of the proposal)	$128,000/ $64,000
PI Chris Kim (Univ. of Minnesota)/ Co-PI Janapa Reddi	Circuit and Architecture Co-Design for Near Threshold Voltage-Based Mobile Application Processors	Univ. of Minnesota (subcontract)	VJ: 50% CK: 50% (the project was on	$100,000/ $43,500

			circuit and architecture co-design, specifically for mobile NTV processors. I was responsible for the architecture half of the proposal)	
PI Janapa Reddi/ Co-PI Sek Chai (SRI)	Resilient Computing Systems Using Deep Learning Techniques	National Science Foundation	VJ: 53% SC: 47% (I was responsible for the resilient architecture piece of the project, while Sek was helping my students with machine learning methods)	$499,959/ $265,000
PI Janapa Reddi/ Co-PI Chris Kim (Univ. of Minnesota)	Feedback-driven resiliency for Near Threshold Systems	National Science Foundation	VJ: 50% CK: 50% (same as previous proposals with Chris, I was responsible for the architecture piece while Chris handled the circuits part of the research)	$192,000/ $96,000

PI Janapa Reddi/ Co-PI Lizy John (UT Austin)	Cross-Layer Solutions for Sustainable and Reliable Computing Solutions	National Science Foundation	VJ: 70% LJ: 30% (I led the vast majority of this research. More specifically, I did the measureme nt based research with my students that led to publishable material and a PhD thesis. Dr. John and I originally explored simulation based analysis on a novel idea with one MS student that was mostly a dead-end.	$300,000/ $214,670

Vijay Janapa Reddi

The University of Texas at Austin
Web Technologies, Mobile and IoT, Computer Architecture, Runtime Systems, Compilers

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Citation indices	All	Since 2011
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h-index	19	17
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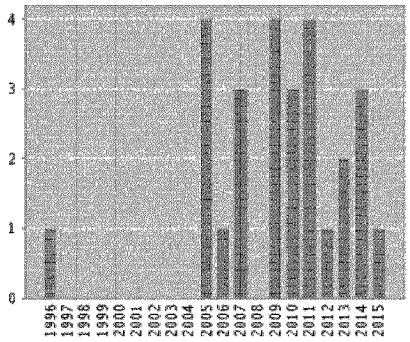

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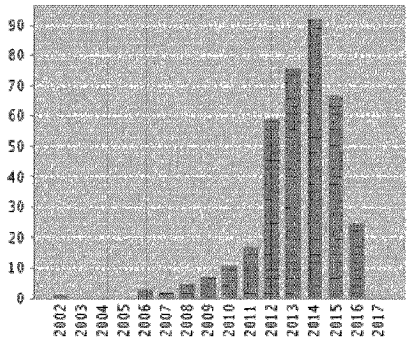

The latest 20 years are displayed.

Results found:	**27**
Sum of the Times Cited [?] :	**365**
Sum of Times Cited without self-citations [?] :	**364**
Citing Articles [?] :	**353**
Citing Articles without self-citations [?] :	**352**
Average Citations per Item [?] :	**13.52**
h-index [?] :	**7**

Sort by: **Times Cited -- highest to lowest**

Page 1 of 3

Use the checkboxes to remove individual items from this Citation Report

or restrict to items published between 1900 and 2017 Go

	2013 ◀	2014	2015	2016	2017 ▶	Total	Average Citations per Year
	76	**92**	**67**	**25**	**0**	**365**	**24.33**
1. **Pin: Building customized program analysis tools with dynamic instrumentation** By: Luk, CK; Cohn, R; Muth, R; et al. Conference: Conference on Programming Language Design and Implementation Location: Chicago, IL Date: JUN 12-15, 2005 Sponsor(s): ACM SIGPLAN ACM SIGPLAN NOTICES Volume: 40 Issue: 6 Pages: 190-200 Published: JUN 2005	62	71	45	10	0	252	21.00
2. **A dynamic compilation framework for controlling microprocessor energy and performance** By: Wu, Q; Reddi, VJ; Wu, YF; et al. Book Group Author(s): IEEE Computer Society Conference: 38th Annual IEEE/ACM International Symposium on Microarchitecture Location: Barcelona, SPAIN Date: NOV 12-16, 2005 Sponsor(s): ACM SIGMICRO; IEEE TC uARCH; Univ Politecn Catalunya; Spanish Minist Sci & Educ; Catalan Govt MICRO-38: Proceedings of the 38th Annual IEEE/ACM International Symposium on Microarchitecture Book Series: INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE, PROCEEDINGS Pages: 271-282 Published: 2005	4	1	1	2	0	19	1.58
3. **PLR: A Software Approach to Transient Fault Tolerance for**							

	Multicore Architectures By: Shye, Alex; Blomstedt, Joseph; Moseley, Tipp; et al. IEEE TRANSACTIONS ON DEPENDABLE AND SECURE COMPUTING Volume: 6 Issue: 2 Pages: 135-148 Published: APR-JUN 2009	3	1	3	1	0	15	1.88
☐ 4.	**Using process-level redundancy to exploit multiple cores for transient fault tolerance** By: Shye, Alex; Moseley, Tipp; Reddi, Vijay Janapa; et al. Conference: 37th Annual IEEE/IFIP International Conference on Dependable Systems and Networks Location: Edinburgh, SCOTLAND Date: JUN 25-28, 2007 Sponsor(s): IEEE Comp Soc TCDCFT; IFIP WG10 4 37TH ANNUAL IEEE/IFIP INTERNATIONAL CONFERENCE ON DEPENDABLE SYSTEMS AND NETWORKS, PROCEEDINGS Book Series: International Conference on Dependable Systems and Networks Pages: 297-306 Published: 2007	2	4	2	1	0	12	1.20
☐ 5.	**Web Search Using Mobile Cores: Quantifying and Mitigating the Price of Efficiency** By: Reddi, Vijay Janapa; Lee, Benjamin C.; Chilimbi, Trishul; et al. Book Group Author(s): ACM Conference: 37th International Symposium on Computer Architecture Location: St Malo, FRANCE Date: JUN 19-23, 2010 Sponsor(s): ACM SIGARCH; IEEE Comp Soc; IEEE TCCA ISCA 2010: THE 37TH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE Book Series: Conference Proceedings Annual International Symposium on Computer Architecture Pages: 314-325 Published: 2010	0	2	1	1	0	11	1.57
☐ 6.	**Voltage Emergency Prediction: Using Signatures to Reduce Operating Margins** By: Reddi, Vijay Janapa; Gupta, Meeta S.; Holloway, Glenn; et al. Book Group Author(s): IEEE Comp Soc Conference: 15th International Symposium on High-Performance Computer Architecture Location: Raleigh, NC Date: FEB 14-18, 2009 Sponsor(s): IEEE Comp Soc Tech Comm Comp Architecture; IEEE Comp Soc; IEEE Intel; hp Invent; Microsoft Res; IBM Res; NSF HPCA-15 2009: FIFTEENTH INTERNATIONAL SYMPOSIUM ON HIGH-PERFORMANCE COMPUTER ARCHITECTURE, PROCEEDINGS Book Series: International Symposium on High-Performance Computer Architecture-Proceedings Pages: 18-29 Published: 2009	0	2	3	1	0	8	1.00
☐ 7.	**High-Performance and Energy-Efficient Mobile Web Browsing on Big/Little Systems** By: Zhu, Yuhao; Reddi, Vijay Janapa Book Group Author(s): IEEE Conference: 19th IEEE International Symposium on High Performance Computer Architecture (HPCA) Location: Shenzhen, PEOPLES R CHINA Date: FEB 23-27, 2013 Sponsor(s): IEEE; IEEE Comp Soc; IEEE Comp Soc TC Comp Architecture; NSF; Chinese Acad Sci (CAS); Intel; Huawei; Sugon; Chinese Acad Sci (CAS), Inst Comp Technol (ICT), State Key Lab Comp Architecture; Chinese Acad Sci (CAS), Inst Comp Technol (ICT); IBM Res; Microsoft Res; Hp; Loongson Technol; Inspur 19TH IEEE INTERNATIONAL SYMPOSIUM ON HIGH PERFORMANCE COMPUTER ARCHITECTURE (HPCA2013) Book Series: International Symposium on High-Performance Computer Architecture-Proceedings Pages: 13-24 Published: 2013	0	1	5	1	0	7	1.75
☐ 8.	**VOLTAGE NOISE IN PRODUCTION PROCESSORS** By: Reddi, Vijay Janapa; Kanev, Svilen; Kim, Wonyoung; et al. IEEE MICRO Volume: 31 Issue: 1 Pages: 20-28 Published: JAN-FEB 2011	2	1	1	2	0	7	1.17
☐ 9.	**Resilient Architectures via Collaborative Design: Maximizing Commodity Processor Performance in the Presence of Variations** By: Reddi, Vijay Janapa; Brooks, David IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS Volume: 30 Issue: 10 Pages: 1429-1445 Published: OCT 2011	0	3	0	2	0	5	0.83
☐ 10.	**Dimetrodon: Processor-Level Preventive Thermal Management via Idle Cycle Injection** By: Bailis, Peter; Reddi, Vijay Janapa; Gandhi, Sanjay; et al. Book Group Author(s): ACM; IEEE; EDAC							

Conference: 48th ACM/IEEE/EDAC Design Automation Conference (DAC) Location: San Diego, CA Date: JUN 05-09, 2011 Sponsor(s): IEEE; Assoc Comp Machinery (ACM); EDAC PROCEEDINGS OF THE 48TH ACM/EDAC/IEEE DESIGN AUTOMATION CONFERENCE (DAC) Book Series: Design Automation Conference DAC Pages: 89-94 Published: 2011	1	3	1	0	0	5	0.83

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27 records matched your query of the 107,000,792 in the data limits you selected.

Budget Council Assessment on Academic Advising, Counseling, and other Student Services for Dr. Vijay Janapa Reddi

This statement on the academic advising, counseling, and other student services for Assistant Professor Vijay Janapa Reddi was prepared by Professor Ross Baldick on behalf of the Budget Council. The statement was prepared following a review of the materials in Dr. Janapa Reddi's tenure dossier, supplemented with information from his annual reports, and an in-depth knowledge of ECE departmental activities.

Undergraduate Academic Advising and Counseling

Dr. Janapa Reddi has actively mentored and advised undergraduate students from freshmen to senior levels, including supervising three undergraduate students who have graduated from UT and subsequently pursued graduate degrees. His approach includes making available to undergraduates the completed systems from graduate research projects, which concretely connects his undergraduate mentoring to his research program. He has also supervised three ECE senior design teams.

He teaches a freshmen-level class (EE319k). He has participated in Eta Kappa Nu (HKN) Psi Chapter's (an ECE honor society at UT Austin) "fireside" chats to provide general student counseling and has mentored three senior design teams (EE464). He has also served as the Faculty Advisor to several upper-division undergraduate students in Computer Architecture and Embedded Processors (CAEP).

Graduate Academic Advising and Counseling

Dr. Janapa Reddi actively participates in graduate student admission, recruitment, and retention activities for Architecture, Computer Systems, and Embedded Systems (ACSES) and Software Engineering and Systems (SES).

Dr. Janapa Reddi currently has six PhD students under his supervision and has graduated two MS students (one co-supervised with Professor Lizy John). The research productivity of his students is very strong, with his first PhD student publishing eight peer-reviewed conference articles under Dr. Janapa Reddi's supervision, and his second PhD student having been made an offer of an assistant professor position at Shanghai Jiao Tong University (SJTU). This is an exceptional record for an assistant professor. Although Dr. Janapa Reddi has not yet graduated a PhD, his second PhD student recently passed his PhD defense and is applying final changes to his dissertation. The student does not intend to graduate until the end of the Fall 2016 semester, but given the quality of his work and him successfully defending his dissertation there is no reason to doubt he will indeed graduate as planned.

In summary, in the areas of academic advising, counseling, and other student services, Dr. Janapa Reddi's performance has been very good, and he has consistently met our department's expectations for his rank.

Summary prepared by Budget Council Member Professor Ross Baldick.

Ross Baldick

Ross Baldick, Professor Department of Electrical and Computer Engineering

Summary on Advising, Counseling and Other Student Services

Vijay Janapa Reddi

1. Advising Undergraduate Students

My approach to mentoring undergraduate students is to strongly encourage them to pursue research early in their academic careers. I have been successful at integrating undergraduate students into research and development at The University of Texas at Austin, and elsewhere. For instance, I have mentored three undergraduate students so far that are actively pursuing graduate school education and research at prestigious institutions.

Peter Bailis was my first undergraduate mentee, and he was very successful under my supervision. Peter published a conference article, "Dimetrodon: Processor-level Preventive Thermal Management via Idle Cycle Injection," at the prestigious Design Automation Conference (DAC). Soon after, he decided to pursue his PhD at the University of California at Berkeley, and graduated recently. Another undergraduate student, Svilen Kanev, also pursued research under my supervision. He also published an article as a second author on "voltage smoothing" that appeared in the prestigious International Symposium on Microarchitecture (MICRO). Moreover, he received 2nd place Male Award as the Computing Research Association's Outstanding Undergraduate for his research. He is currently pursuing his PhD at Harvard University, and is expected to graduate in the coming year. Tri Nguyen worked with me on accelerating biomedical applications using hardware accelerators during his junior year. He is pursuing a PhD at Princeton University.

I provide quality mentoring to my students; therefore, each year I pick one student to mentor. My goal is to train the student for two to three years until they are successfully off to graduate school. Currently, I am training James Orr on machine learning techniques for computing on Big Data.

I believe an important reason that students under my supervision are successful at research is because of my *hands-on and practical engineering-oriented approach to training undergraduates.* I make the systems we develop in my research lab available to my undergraduate students. For instance, in a prior NSF project we performed the instrumentation of commercial computer systems for measuring the energy/power of real-world applications. After the research project finished, I transformed the instrumentation platform into a "hands-on" platform for undergraduate research projects. The power measurement infrastructure shown in Figure 1 allows students to easily study the interaction between changing compiler optimizations and the consequential impacts on the energy/power consumed by the system. We have similar infrastructure for studying reliability.

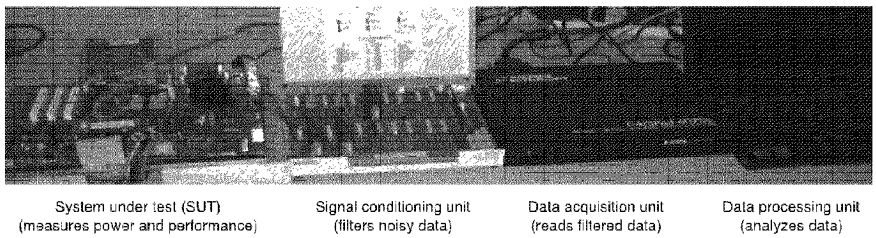


Figure 1: Example of the hands-on system I use to train my undergraduate students

In addition, I have also supervised undergraduate research by mentoring ECE senior design teams. Senior design projects in ECE span a full academic year. I have met with students weekly to provide technical mentoring and mentoring of their communication and organizational skills. Teams include:

- 2015 – Present: "A Smart Ambient Lighting System" – This project involves the design and engineering of a smart ambient lighting system to address personal health, home security, and productivity. The system will offer an internet-of-things solution for automated home and commercial lighting to improve the wellbeing of the users.

- 2014 – 2015: "ReddiSphere" – is a system that phone application developers could use to accurately test their applications with stimuli in a virtual environment.

- 2012 – 2013: "Ray Tracing with Texas Instruments multi-core Digital Signal Processor" - This project designed a low powered portable device capable of parallel programming.

2. Advising Graduate Students

In my view, the process of getting a Ph.D. is pretty typical. The process involves three principal steps: (a) students must first learn to identify fundamental research problems by developing a thorough understanding of state-of-art literature; (b) students must develop a strong technical background that enables them to propose independent and innovative solutions to those challenging problems; (c) students must publish extensively at the Tier-1 conferences and journals to gain credibility and recognition for their work. Practically all students follow this process to earn a PhD.

Getting a PhD under my supervision requires more than following those principal steps. In addition, I encourage my students to develop their own unique research style, and support them in teaching others what they know – including me. I prefer not to impose my ideas. Instead, I help my students develop their own ideas. I often see myself as a facilitator of their research. I take this role because I believe that if students learn to take ownership of their work, they will lead it in new directions that even I cannot anticipate. By taking such an approach, my lab pursues unconventional research.

My student's high research productivity is evidence that my approach to graduate supervising works. Yuhao Zhu, my first PhD student, has published eight peer-reviewed top-tier conference articles in mobile computing over five years. Prior to our foray into this topic, mobile computer architecture was a largely overlooked topic in the Computer Architecture community. Over the recent years, Yuhao and I have actively worked on publishing papers to establish the area. For his outstanding research contributions, Yuhao received the Google PhD fellowship, which is a very competitive and prestigious fellowship award given to the very best students that have made impactful contributions.

Furthermore, my second PhD student in the pipeline, Jingwen Leng, who is getting ready to graduate, has also produced outstanding work. His unique contributions to the community have been in developing a research infrastructure that enables the rest of the community to do research. He developed GPUWattch, which is used by over 5,000 people (based on downloads) in the Computer Architecture community. Jingwen's research record is so outstanding he has landed an academic position as an assistant professor at a top engineering school – Shanghai Jiao Tong University (SJTU).

In general, I teach my students to not only produce research publications, but also build artifacts that others can use to evaluate and build upon. I strongly believe that in doing so, students experience a greater responsibility for their research, and it shapes the problems they chose to solve. These qualities are key to helping our students become leaders, not simply graduates with a PhD degree.

3. Advising Student Organizations

In addition to working directly with students, I have worked with Eta Kappa Nu (HKN) Psi Chapter, which is the Electrical and Computer Engineering Honor Society at The University of Texas at Austin. Over the years, I have attended their "fireside" events where students are allowed to ask their professors anything they would like to know about mentoring, teaching, research, etc. I support these activities by taking part in them because I believe that students should have unrestricted access to their professors. By taking part in these activities, I have helped students understand the road to graduate school and the opportunities that they have at The University of Texas at Austin to go beyond the classroom and take part in academic leadership activities, and take part in sponsored research.

Many students have sought me for advice after the fireside activities, and I have helped them not only earn undergraduate research positions, but also earn internship positions in industry (e.g., Intel).

Table 1. Summary of Academic Advising

Metric	Value
Student organizations advised	1
Undergraduate ***researchers*** supervised	3
PhD students completed *	0 (0 sole advisor)
MS students completed *	1.5 (1 sole advisor)
PhD students in pipeline (as of 09/2016)*	6 (6 sole advisor)
MS students in pipeline (as of 09/2016)*	0 (0 sole advisor)

Table 2. Completed Graduate Students Supervised by Candidate

Student ***Name***	Co-Supervisor	Degree	Start Date	Graduation Date	Placement
Aditya Srikanth		MS	08/2011	05/2013	NVIDIA
Ankita Goel	Lizy John	MS	08/2011	08/2013	VMware

Budget Council Assessment of Service to the University and to the Nation, State, and Community

Vijay Janapa Reddi

Summary

Professor Janapa Reddi's service record is exceptionally strong both within the department and in the broader scientific community. He has been a solid citizen and already has a high national and international profile. In terms of overall service, he compares very favorably with colleagues who successfully achieved tenure in our department.

Service to the Nation, State, and Community

Professor Janapa Reddi is extremely active and visible in the scientific community. Most notably, he has already served on over 15 technical program committees for key conferences in his area (such as ISCA, HPCA and CGO). He is now taking on more leadership roles, including serving as General Chair for the International Symposium on Code Generation and Optimization (CGO), 2017, organizing a variety of tutorials at leading conferences and serving as guest editor for IEE Micro special issues.

Professor Janapa Reddi has also been active in educational activities in local communities, including teaching a course for 100+ Intel engineers, giving multiple presentations at both Intel and AMD in Austin, as part of his consulting activities. He has also given a presentation on the future of mobile computing to STEM students in Texas. Most noteworthy is his effort in developing a workshop on Internet of Things, with associated hands-on activities, targeted towards middle-school students. Through UTeach, his effort is expected to receive a nation-wide audience in the coming years.

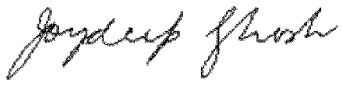
Service to the University

Since arriving at UT Austin, Professor Janapa Reddi has performed significant service to the University given his rank. Within the ECE Department, he has served as a member of the ECE Graduate Student Admissions Committee since he joined the faculty in 2011. He has twice served on the demanding Faculty Recruiting Committee, and was a key member of the Technology for Teaching Committee, being very attuned to emerging technologies for learning and teaching. He has also been very active in the Computer Architecture group, mentoring and counseling both undergraduate and graduate students.

Basis for Evaluation

This Budget Council assessment of Professor Janapa Reddi's service is based on a thorough evaluation of the materials put together by the candidate for promotion to associate professor, combined with knowledge of the candidate's service activities.

Prepared by Electrical and Computer Engineering Budget Council member



Joydeep Ghosh 1 August 2016

Service to the University and to the Nation, State and Community

Vijay Janapa Reddi

1. Service to the University

Service to the University has been a central aspect of my academic role in achieving and strengthening the University's mission. My service activities are enumerated below:

UNIVERSITY COMMITTEE ASSIGNMENTS:

Departmental-	Member, Faculty Recruiting Committee	2015
	Member, Technology in Teaching Committee	2014
	Member, Faculty Recruiting Committee	2013
	Graduate Student Admissions Committee	2011- Present

2. Service to the Nation

I strongly believe in contributing to the development of our nation, and to this end, I have proactively volunteered to lead many different organizational positions. My roles range from leading a conference's general organization to supervising the technical program to handling finance, publications, and other organizational duties. Over the years, I have covered practically all aspects involved in organizing and running a conference. Furthermore, I have organized tutorials and workshops that bring together experts in the field to brainstorm issues facing computer system design. When I lead such activities, I am in the pursuit of not only conducting technical research, but in laying the foundations that are much needed to enable the rest of the community.

- General Chair, Intl. Symp. on Code Generation and Optimization (CGO 2017)
- Finance Chair, Intl. Symp. on Code Generation and Optimization (CGO 2015)
- Program Committee,
  - Intl. Symp. on Computer Architecture (ISCA 2014)
  - High Performance Computer Architecture (HPCA 2012, 2014, 2015)
  - Microarchitecture (MICRO 2013,2014)
  - Principles and Practice of Parallel Computing (PPoPP 2013, 2015)
  - Code Generation and Optimization (CGO 2013, 2014)
  - Parallel Architectures and Compilation Techniques (PACT 2013)
  - Workload Characterization (IISWC 2012, 2013, 2016)
  - Parallel & Distributed Processing (IPDPS 2012)
  - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2012)
- Program Chair, Intl. Symp. on Code Generation and Optimization (CGO 2014)
- Guest Editor,
  - IEEE Micro Special Issue on Reliability-Aware Microarchitecture Design (2013),
  - IEEE Micro Special Issue on Internet of Things (2016)
- Local Arrangements Chair,
  - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2013)
  - Workshop on Silicon Errors in Logic - System Effects (SELSE 2015, 2016)
- Publications Chair, Intl. Symp. on Workload Characterization (IISWC 2013)
- Organizer
  - Tutorial on Tools for Mobile Computer Architecture (MobiTools 2016)

  - Tutorial on Simulation and Analysis Engine (ISCA 2016, ASPLOS 2016, HPCA 2016, ICS 2016, IISWC 2015, ISPASS 2015)
  - Workshop on Resilient Architectures (WRA 2013–2010)
- Steering Committee, Intl. Symp. on Code Generation and Optimization (CGO)

3. Service to the State

I have been involved in state-level educational development. I have given many invited presentations on my sponsored research at local industries over my tenure-track position to disseminate state-of-the-art findings.

I have been involved with companies, such as AMD and Intel because they play a vital role in the state by employing many different students from UT Austin and the Austin community. I have given presentations on my research and taught courses at these companies to help educate their employees on state-of-the-art advances in computing. For instance, in Summer 2014 I taught a course to over 150 Intel engineers in Austin on the "Internet of Things." For completeness, I have included the details of these talks in my Curriculum Vitae.

In addition, I have shared my knowledge at the IEEE Texas Workshop on Integrated System Exploration (WISE) that was held at Rice University on May 6th 2016. I was invited to give a presentation on the future of mobile computing. There were over 100 attendees. The program is targeted specifically at Texas students, encouraging STEM diversity and underrepresented minorities to participate. The goal is to motivate students to understand computing's future, and the numerous challenges and opportunities for future research and development.

4. Service to the Community

I have been working for the past two years to develop a new workshop called ``Connect the World with the Internet of Things (IoT),'' designed to help generate the interest of Austin's middle and high school students' in one of the STEM disciplines by showing them the power and simplicity of today's mobile technology. The program exposes them to a full day of activities involving Intel's Arduino Galileo device for the IoT.

To develop the workshop further into a full-fledged classroom activity, over the past two years, I have become responsible for developing a series of 16 hands-on inquiry-based lessons that introduce upper elementary students to computer science. The course teaches students programming and logic through a unique hands-on and practical approach, engaging students by having them design and develop code that animates objects they control using Arduino-based computers, LEDs, resistors, servos, etc. I develop this program with UTeach, which makes it available through their outreach efforts to the community: https://outreach.uteach.utexas.edu/csp

The completed first eight lessons were assessed for effectiveness in a pilot program over Summer 2015. Data was collected on the course's effectiveness and attitudinal impact on 50 students, of which 89% qualified for federal free and reduced meals and 51% were Hispanic. The course was included as a pilot in Fall 2015, as part of the local Austin Independent School District (AISD) middle school curriculum—offered to 6th graders.

After further evaluation and revisions of the curriculum under development, the lessons will be disseminated through the nationally recognized UTeach Program at the University of Texas. UTeach's academic network includes over 44 universities nationwide. Therefore, the completed lessons will be taught across the nation.

Budget Council Assessment of Honors and other Evidence of Merit or Recognition, Including Contracts and Grants

Basis for this Evaluation: This assessment is based on a comprehensive evaluation of the promotion materials provided by Dr. Janapa Reddi.

Dr. Janapa Reddi has been very successful in seeking external funding for his research. He has participated overall in attracting $2,403,959 of which $1,810,670 is his share. The funding comes from diverse sources including three peer reviewed competitive grants from the National Science Foundation, support from the Semiconductor Research Corporation (an industry consortium), and multiple industry gifts from Google, Intel, and AMD, which are companies that would draw in his research work. Overall this is a balanced funding portfolio including grants where he is serving as the PI as well as others where he is collaborating with colleagues both at UT and University of Minnesota.

Dr. Janapa Reddi has received many awards throughout his career, including several best paper awards and "Top Picks" designations. The two most prestigious research awards while in rank are

- Top Picks Honorable Mention in Computer Architecture, *IEEE Micro* 2016
- Most Influential Paper Award in *Programming Language Design and Implementation* (PLDI) ACM SIGPLAN 2015

In fact, over the years, three of his papers have received a "Micro Top Pick" designation and one an "honorable mention." This is significant in that these papers are selected after publication from the best works in the community that year. The second award recognized an early work (2005) "Pin building customized program analysis tools with dynamic instrumentation" on which he was a co-author, and represents a retrospective look at works that have been influential in the community.

In addition, he has recently been awarded the IEEE Technical Committee on Computer Architecture (TCCA) Young Computer Architect Award (2016). The previous winners of this award, which is administered by the IEEE Computer Society, are particularly distinguished faculty who are very well known young stars in the community. As indicated in the award description, "The winner of the award will be someone who has made an outstanding, innovative research contribution or contributions to Computer Architecture."

In summary, overall Dr. Janapa Reddi has not only been successful in raising funding for his research group, but is getting substantial recognition in top venues in his community, including recognition amongst the top young stars in his field.

Prepared by the ECE Department Budget Council Member:

Gustavo de Veciana

Prof. Gustavo de Veciana

Honors and Other Evidence of Merit or Recognition, Including Contracts & Grants

Vijay Janapa Reddi

1. Young Faculty Awards

I received the IEEE TCCA Young Computer Architect Award (2016) "in recognition of outstanding research contributions in mobile computing and resilient architectures." The award recognizes outstanding research contributions by an individual in the field of Computer Architecture, who received his/her PhD degree within the last 6 years. It is administered by the IEEE Computer Society.

I am also the recipient of the National Academy of Engineering's Gilbreth Lectureship honor. The citation reads "for outstanding contributions to the field of electrical and computer engineering and his presentation of the lecture on energy efficiency and mobile computing." The Gilbreth Lectures were established in 2001 by the Council of the National Academy of Engineering as a means of recognizing outstanding young American engineers and making them more visible to the NAE membership. Recipients of the lectureships are nominated from the Frontiers of Engineering program and have the opportunity to make presentations at NAE's fall Annual Meetings and spring National Meetings. The Gilbreth Lectureships are named in honor of Lillian Gilbreth, the first woman elected to the National Academy of Engineering (1965) and a pioneer in the field of Human Factors.

In addition to these significant awards, I have also received numerous other honors and awards over the course of my professional career. These are listed under the "Honors and Awards" section of my Curriculum Vita.

In general, the key theme for all my awards has been in the establishment of mobile computer architecture research within the community and for out-of-the-box research solutions that involve tight coupling between the hardware and software layers, without breaking programmability.

2. Research Awards

I have been honored with technical awards recognizing my research contributions. These honors include the following:

- Top Picks Honorable Mention in Computer Architecture, *IEEE Micro*, 2016 – IEEE Micro collects some of this year's most significant research papers in computer architecture based on novelty and potential for long-term impact. Any computer architecture paper (not a combination of papers) published in the top conferences of 2015 (including MICRO-48) is eligible. IEEE Micro also distinguishes a number of papers as IEEE Micro Top Pick Honorable Mentions.

- SIGPLAN Most Influential Paper Award, *Programming Language Design and Implementation (PLDI)*, 2015 -- Presented annually to the author(s) of a paper presented at the PLDI held 10 years prior to the award year. The award includes a prize of $1,000 to be split among the authors of the winning paper. The papers are judged by their influence over the past decade.

- Google Faculty Research Award, *Google*, 2012, 2013, 2015 -- Google Research Awards are one-year awards structured as unrestricted gifts to universities to support the work of world-class full-time faculty members at top universities around the world, funded based on competition.

- I have received best paper awards at HPCA and MICRO, which are tier-one conferences (see CV).

3. Research Funding

I have been successful in receiving funding from various competitive sources, including the National Science Foundation (NSF), Semiconductor Research Corporation (SRC) and the industry (e.g. Google Faculty Research Awards).

I have been successful at raising funding for different types of research projects, ranging from mobile computing to hardware reliability—not just one type of research theme. For instance, from NSF I have both mobile computing funding, as well as computer systems' reliability funding. Similarly, with industry funding I have raised funding for mobile computing involving end-user quality-of-experience, as well as conducting research that involves power, thermal and performance modeling.

In addition, I have also been successful in sourcing money under different types of requirements. For instance, industry funding typically has a more practical aspect to the research, whereas NSF and SRC expect long-term research visions. I have demonstrated that I can manage these differences well.

4. Invited Talks

Over the past five years, I have given numerous invited talks. As listed individually on my CV, I have given almost 50 talks at leading conferences, symposiums, and universities. In addition to giving talks, I have also been invited to write position articles in prestigious and heavily read technical journals and magazines. Recently I have been asked to describe the future of Mobile Web Computing for ACM Queue. The article will be featured in the upcoming edition, available towards the year end.

LETTERS RECEIVED – VIJAY JANAPA REDDI

A minimum of four review letters should be listed *alphabetically* with affiliation, etc.

Name of reviewer, rank or title, department, university	David H. Albonesi Professor School of Electrical and Computer Engineering Cornell University
Brief statement of expertise and reason for selection*	Expert in Computer Architecture; IEEE Fellow; Professor in Major research Institution
Other relevant information**	Editor-in –Chief of Major Publication in field
Nominated by	Budget Council
Date letter received	August 14, 2016

Name of reviewer, rank or title, department, University	David I. August Professor Department of Computer Science Princeton University
Brief statement of expertise and reason for selection*	Expert in Compiler and microarchitecture; Professor in Major research Institution
Other relevant information**	
Nominated by	Budget Council
Date letter received	August 7, 2016

Name of reviewer, rank or title, department, university	Thomas M. Conte Professor Joint appointment – School of Computer Science and School of Electrical and Computer Engineering Georgia Tech
Brief statement of expertise and reason for selection*	Expert in Compilers and Computer Architecture; IEEE Fellow; Professor in Major research Institution
Other relevant information**	Outgoing President of IEEE Computer Society
Nominated by	Budget Council
Date letter received	August 7, 2016

Name of reviewer, rank or title, department, university	Chita R. Das Distinguished Professor and Interim Head Department of Computer Science and Engineering The Pennsylvania State University
Brief statement of expertise and reason for selection*	Expertise in Computer Architecture, Performance Evaluation, Parallel and distributed computing; IEEE Fellow
Other relevant information**	
Nominated by	Candidate
Date letter received	August 5, 2016

Name of reviewer, rank or title, department, university	Christos Kozyrakis Associate Professor – Electrical Engineering and Computer Science at Stanford Professor – Computer Science at EPFL Stanford University/EPFL
Brief statement of expertise and reason for selection*	Expert in Computer Architecture; IEEE Fellow; Professor in Major research Institution;
Other relevant information**	ACM Maurice Wilkes Award
Nominated by	Candidate
Date letter received	August 13, 2016

Name of reviewer, rank or title, department, university	Scott A. Mahlke Professor and Associate Chair Electrical Engineering and Computer Science Department University of Michigan
Brief statement of expertise and reason for selection*	Expert in Compilers and Computer Architecture; IEEE Fellow; Professor in Major research Institution
Other relevant information**	
Nominated by	Candidate
Date letter received	July 22, 2016

Name of reviewer, rank or title, department, university	Onur Mutlu Professor Department of Computer Science Swiss Federal Institute of Technology Zurich
Brief statement of expertise and reason for selection*	Expert in Computer Architecture; Professor in Major research Institution
Other relevant information**	Professor at Carnegie Mellon University until May 2016
Nominated by	Budget Council
Date letter received	August 21, 2016

Name of reviewer, rank or title, department, university	Josep Torrellas Saburo Muroga Professor Department of Computer Science University of Illinois at Urbana-Champaign
Brief statement of expertise and reason for selection*	Expert in computer architecture, parallel processing, and resilience ; IEEE and ACM Fellow; Professor in Major Research Institution
Other relevant information**	Illinois Professor for 24 years
Nominated by	Candidate
Date letter received	August 8, 2016

Name of reviewer, rank or title, department, university	Matt Welsh Lead, Chrome Cloud Team Google, Inc.
Brief statement of expertise and reason for selection*	Renowned Google researcher and engineer; Expert on mobile computing, networking, distributed systems and Web technologies
Other relevant information**	Former Harvard Professor; Lead of Google Chrome Cloud Team
Nominated by	Candidate
Date letter received	July 27, 2016

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
Cockrell School of Engineering

1616 Guadalupe St. • UTA Building, 7th Floor • Austin, Texas 78701
http://www.ece.utexas.edu/

June 23 2016

Dear Prof. Das:

The Department of Electrical and Computer Engineering is considering Dr. Vijay Janapa Reddi for tenure and advancement in rank to the position of associate professor at the University of Texas at Austin. We would appreciate your candid assessment of his scholarly contributions to assist our decision-making process. Excellent teaching is an important criterion for promotion, but our evaluation of teaching is being carried out separately, and we are asking you only for information about his scholarly distinction.

Copies of Dr. Janapa Reddi's curriculum vitae and several recent papers are posted at the following location. You can access them at:https://www.ece.utexas.edu/promotions/vijay-janapa-reddi-2016 using the following credentials:

Username: reddi1
Password: K2Ku8m

We would appreciate your opinions regarding Dr. Janapa Reddi's major engineering and/or scientific contributions. In preparing your assessment, please consider the following questions:

1. Do you know Dr. Janapa Reddi, and if so, for how long and under what circumstances?
2. What are the original, innovative, and/or important contributions that he has made in his field of research? Have his publications influenced the thinking of, or the methods used by, others in your field?
3. How would you assess Dr. Janapa Reddi's development compared with others in his cohort at research-intensive universities?
4. What is your perspective on Dr. Janapa Reddi's promise for further professional growth and leadership?

We would be grateful for any additional comments you might have. The more specific you can be in your comments, the more helpful your evaluation will be.

Under the laws of the State of Texas, Dr. Janapa Reddi has the right to request to see any materials in his personnel file, including your letter. Members of our faculty and internal review committees who see your letter as part of the promotion process will hold the comments you make in confidence, however.

For your comments to receive full consideration, we will need to receive a signed letter from you no later than August 1, 2016. It is not necessary for you to send us a hard copy of your letter, an electronic or scanned version is sufficient, provided your institutional letterhead and your signature are included. In addition, please enclose a copy of a short version of your curriculum vitae (preferably no longer than two pages) or the URL for your web site where we may obtain this information. If you have questions, please call me at the number given on the letterhead.

Thank you for your time and assistance with this important matter. As faculty members, we realize that the amount of time required to do a thoughtful review is considerable.

Sincerely,

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

List of Materials Sent to Outside Reviewers

Vijay Janapa Reddi
Electrical and Computer Engineering
The University of Texas at Austin

1) CV
2) Five Significant Publications
3) Research Statement
4) Teaching Statement

Five Most Significant Publications (in Rank)
Prof. Vijay Janapa Reddi

Dept. of Electrical and Computer Engineering,
The University of Texas at Austin,
vj@ece.utexas.edu

1. S. Campanoni, T. Jones, G. Holloway, **V. Janapa Reddi**, G. Wei, D. Brooks. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing." in IEEE/ACM International Symposium on Code Generation and Optimization (CGO), pp.84-93, March, 2012. http://dx.doi.org/10.1145/2259016.2259028

2. Y. Zhu, **V. Janapa Reddi**. "High-Performance and Energy-Efficient Mobile Web Browsing on Big/Little Systems," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.13-24, February 2013. http://dx.doi.org/10.1109/hpca.2013.6522303

3. J. Leng, T. Hetherington, A. ElTantawy, S. Gilani, N. Kim, T. Aamodt, **V. Janapa Reddi**. "GPUWattch: Enabling Energy Optimizations in GPGPUs," in ACM/IEEE International Symposium on Computer Architecture (ISCA), vol 41(3), pp.487-498, June 2013. http://dx.doi.org/10.1145/2485922.2485964

4. Y. Zhu, **V. Janapa Reddi**. "WebCore: Architectural Support for Interactive Mobile Web Browsing," in ACM/IEEE International Symposium on Computer Architecture (ISCA), pp.541-552, June 2014. http://dx.doi.org/10.1109/isca.2014.6853239

5. J. Leng, Y. Zu, V. **Janapa Reddi**. "GPU Voltage Noise: Characterization and Hierarchical Smoothing of Spatial and Temporal Voltage Noise Interference in GPU Architectures," in IEEE International Symposium on High Performance Computer Architecture (HPCA), pp.161-173, February 2015. http://dx.doi.org/10.1109/hpca.2015.7056030

BC

School of Electrical and Computer Engineering

David H. Albonesi
Professor

Computer Systems Lab
333 Rhodes Hall
Ithaca, NY 14853 USA

607 254-5473 Tel
607 255-9072 Fax
albonesi@csl.cornell.edu

August 14, 2016

Professor Ahmed Tewfik
Chair, Department of Electrical and Computer Engineering
The University of Texas at Austin
Austin, TX 78701

Dear Professor Ahmed:

I enthusiastically support the promotion of Professor Vijay Janapa Reddi to Associate Professor with tenure. I first became familiar with his work on reliability while he was a Ph.D. student at Harvard, and I have closely followed his research since he joined UT as we both work in computer architecture. Professor Janapa Reddi is a rising star in the computer architecture community and in my mind he clearly deserves tenure.

Architects can no longer simply ride the CMOS technology scaling curve for performance improvements, and energy and reliability issues have risen in prominence with technology scaling. Professor Janapa Reddi has distinguished himself as one of the foremost researchers in cross-layer solutions—combining hardware, compilers, and applications—to increase computer system performance within increasingly stringent energy and reliability constraints. Professor Janapa Reddi's contributions to the field of computer systems, which span mobile computing to datacenters to supercomputing as well as multiple levels of the system stack, are unusually broad and deep for his level of seniority; very few tenure cases that I review have demonstrated impact across the broad research communities of ISCA/MICRO/HPCA, CGO, PLDI, and ICS.

Overall, I am impressed by the strength of Professor Janapa Reddi's research program: his level of funding, recognition for his research, and influential publications. Professor Janapa Reddi's funding level is quite strong, with four NSF grants complemented by significant industry funding from SRC, Intel, Google, and AMD. The Intel Early Career and Google Faculty Research awards are both highly competitive and indicate the strong industry interest in Professor Janapa Reddi's research. His TCCA Young Computer Architect Award is particularly prestigious, since only one award is given across the field each year. This puts Professor Janapa Reddi in the company of an elite group of young computer architecture researchers: past awardees Onur Mutlu, Karthikeyan Sankaralingam, Luis Ceze, Engin Ipek, and Ron Dreslinski.

Professor Janapa Reddi's publication record since joining UT is top-notch. He has published two papers in ISCA, five in MICRO, and three in HPCA. These three conferences are the best in computer architecture, and more prestigious and competitive than journals. Moreover, he has published in PLDI and CGO, which are similarly competitive and prestigious; in other reputable conferences such as ISLPED, ISPASS, and ICS; and in several journals. His two Synthesis Lectures in Computer Architecture (one published and one in progress) are another indication of his strong reputation. Overall, this is an outstanding record of achievement.

The only possible perceived weakness in Professor Janapa Reddi's case might be the lack of an NSF CAREER Award, but I do not consider this a necessary condition for tenure, and the TCCA Young Computer Architect Award more than makes up for it.

Professor Janapa Reddi's promotion case reminds me of that of Professor Tom Wenisch, whose broad and deep contributions to the field earned him tenure at Michigan a number of years ago. His impact is similar to Professors Engin Ipek and Karthikeyan Sankaralingam, who received tenure at the University of Rochester and the University of Wisconsin-Madison, respectively, and like Professor Janapa Reddi won the TCCA Young Computer Architecture Award.

Given his contributions and reputation, I am confident that Professor Janapa Reddi would receive tenure here at Cornell, and I strongly support his case for promotion.

Sincerely,

David H. Albonesi

My bio and CV can be found at http://csl.cornell.edu/~albonesi.

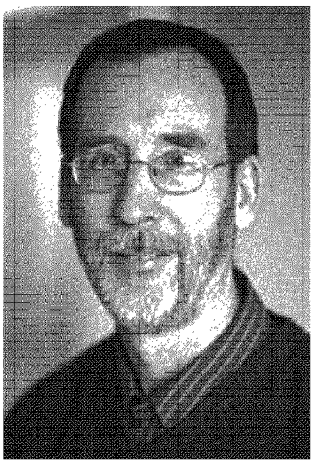
Jilda Gayle

From: David Albonesi <dha7@cornell.edu>
Sent: Sunday, August 14, 2016 9:08 PM
To: Bearden, Carole A
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: Promotion Reference letter - Vijay Janapa Reddi
Attachments: albonesi-letter.pdf; Untitled attachment 00015.htm

Attached is my letter. My apologies for the delay.

Dave

Computer Systems Laboratory



David H. Albonesi
Professor

Computer Systems Laboratory
School of Electrical and Computer Engineering
Cornell University
333 Rhodes Hall
Ithaca, NY 14853
(607) 254-5473
albonesi at csl.cornell.edu

Professor David Albonesi joined the Computer Systems Laboratory in 2004 after serving on the faculty of the University of Rochester. His current research interests include adaptive and reconfigurable multi-core and processor architectures, power- and reliability-aware computing, and energy-efficient smart buildings. In addition to his academic experience, he has ten years of industry experience as a technical manager, computer architect, and chip designer at IBM and Prime Computer.

Dr. Albonesi is a Fellow of the IEEE, and has received the National Science Foundation CAREER Award, three IBM Faculty Awards, three IEEE Micro Top Picks paper awards, and the Michael Tien '72, Ralph S. Watts '72, and Ruth and Joel Spira Excellence in Teaching Awards. He serves on the Editorial Board of IEEE Computer, and was Editor-in-Chief of IEEE Micro from 2007-10. Professor Albonesi was General co-Chair of the 42nd International Symposium on Microarchitecture and Program Chair of the 42nd International Symposium on Computer Architecture. He is a graduate field member of ECE and CS, and teaches courses ranging from freshman-level introductory computing to advanced graduate topics in computer systems.

His MOOC, The Computing Technology Inside Your Smartphone, first launched on EdX in March 2015 and ran for a second time in Summer 2016.

Selected publications

Characterizing the Benefits and Limitations of Smart Building Meeting Room Scheduling, A. Majumdar, Z. Zhang, and D.H. Albonesi, *7th International Conference on Cyber-Physical Systems*, April 2016.

Energy-Comfort Optimization using Discomfort History and Probabilistic Occupancy Prediction, A. Majumdar, J.L. Setter, J.R. Dobbs, B.M. Hencey, and D.H. Albonesi, *5th International Green Computing Conference*, November 2014.

Flicker: A Dynamically Adaptive Architecture for Power Limited Multicore Systems, P. Petrica, A.M. Izraelevitz, D.H. Albonesi, and C.A. Shoemaker, *40th International Symposium on Computer Architecture*, June 2013.

Energy-Aware Meeting Scheduling Algorithms for Smart Buildings, A. Majumdar, D.H. Albonesi, and P. Bose, *4th ACM Workshop on Embedded Systems for Energy-Efficiency in Buildings*, November 2012.

ReMAP: A Reconfigurable Architecture for Chip Multiprocessors, M.A. Watkins and D.H. Albonesi, *IEEE Micro*, Special Issue on the Top Picks from the Computer Architecture Conferences, January/February 2011.

Last Update: July 2016

BC

PRINCETON UNIVERSITY

David I. August
Professor of Computer Science

35 Olden Street
Princeton, New Jersey 08540
T 609.258.2085 F 609.964.1699
august@princeton.edu
http://august.princeton.edu/

Dear Dr. Ahmed Tewfik:

I am writing to you in response to your letter requesting a candid assessment of Dr. Vijay Janapa Reddi's scholarly achievements. Dr. Janapa Reddi is well-known in our community for his research in computer architecture and software design. I have known him for many years (since roughly 2005), not only through his work, but also from personal interactions at various events.

Impact

Dr. Janapa Reddi has already significantly influenced the thinking of and methods used by others in my field. In terms of new methods, his contributions to the field through the Pin and GPUWattch tools are significant. Pin and GPUWattch are both extremely popular, widely used tools that have enabled many new explorations in our field. With so many researchers using these tools in so many different ways, I don't think it possible to know the full extent of their impact. Pin's impact was recognized formally by PLDI (the top conference in programming language practice) with a "Most Influential Paper" award, an award decision made with a full decade's worth of perspective. More personally, my group and I have used Pin to study problems in computer reliability and performance. Its power and ease-of-use enabled us ask and answer important questions, significantly improving our work and even making some of our past explorations possible.

Beyond new methods, Dr. Janapa Reddi has produced numerous original and innovative ideas, ideas which he has shepherded into practical application. I don't think any single tenure letter will quite capture his work with both the breadth and the depth it deserves, so I will instead focus on my favorite two areas of his work.

Reliable and Efficient Computing

The drive for power and energy efficiency in computing systems means, among other things, a reduced supply voltage. As this supply voltage decreases, what was once just a fluctuation in supply voltage becomes a voltage emergency potentially impacting the correctness of computation. Rather than accept more conservative and less efficient designs that eliminate voltage emergencies, Dr. Janapa Reddi has pioneered the effort to enable aggressive designs by handling voltage emergencies using a software-assisted, hardware-guaranteed approach.

That this line of research would produce anything of value is counter-intuitive. Since power and voltage emergencies demand an immediate response, one would not expect software assistance to play any useful role. Nevertheless, Dr. Janapa Reddi saw something others did not. The key breakthrough involves a hybrid between a hardware system that has emergencies, handled suboptimally, and a software system that optimizes the system with the goal of reducing these future suboptimal hardware responses. The beauty of this hybrid system is in its leveraging of both the quick reflexes of hardware and the more global perspective and control available through software.

Beyond this initial idea, Dr. Janapa Reddi has skillfully addressed many challenges to make it more practical and applicable. These challenges include integration with commodity dynamic voltage and frequency scaling systems, extending to multicore, and mapping to embedded systems.

The impact of Dr. Janapa Reddi's research in this one area is significant. Two of his papers have been recognized by best paper awards, both at Tier I conferences, and two of his papers appear as IEEE Micro "Top Picks", arguably one of the most prestigious honors a paper in our field can receive. To put this in context, in this one area of research, Dr. Janapa Reddi's work has received more academic recognition than the majority of researchers in our field have received in total. On top of this, Dr. Janapa Reddi's work in this area has been recognized by keynote invitations, an invitation to edit a special issue on reliability-aware design, and a "Synthesis Lecture" (essentially an invited book).

HELIX

I note that the Dr. Janapa Reddi's tenure case information page lists five publications, including "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing". This one, listed first, is not mentioned explicitly in Dr. Janapa Reddi's research statement. Nevertheless, I consider this work to be very significant as it represents progress in an area with a many decades long record full of failures. This work is also closest to my own, so I am in an excellent position to comment upon it.

In my opinion, the problem Dr. Janapa Reddi and his coauthors chose to address in this work remains the most important problem in computer architecture today. Truth be told, the move to multicore was forced. Microprocessor manufacturers, unable to improve single processor performance at the historical rate we came to expect, turned to multiple cores as a means to create value from the continued increase in transistor count. Unfortunately, for the vast majority of applications, multicore offers little performance gain. Worse, with multicore, no longer do uniprocessor and multiprocessor applications get faster with each processor product generation. Instead, now the job of making computers faster has fallen to programmers. If, as some say, computer science is about abstraction, the step backward that requires the programmer to explicitly utilize core resources in the processor architecture in order to make it perform ranks it among the top failures of computer science. The effects of this failure are real. In the sciences, for example, studies have shown that researchers are generally unable to make good use of multicore, dramatically slowing the pace of scientific discovery.

While some advocate new programming languages and others advocate parallel library building blocks as solutions to the multicore problem, only automatic solutions that work for existing codes do not simply push the problem elsewhere. Automatic parallelization of general purpose legacy codes for multicore processors is an area many have long considered effectively impossible. I respect Dr. Janapa Reddi for choosing to make a contribution on such an important and challenging problem, and I respect him even more for putting forward a successful approach.

When my group stated work in the area about a decade ago, we were warned by more than a few to turn away lest we ruin our careers. For many years, we knew of no other group "crazy enough" to dedicate itself exclusively to this "fool's errand". Even today, when publishing demonstrable progress, our results are often met with skepticism, disbelief, and dismissal. Naturally, in 2012, we felt a great sense of relief with the publication of a truly significant and successful independent work in this area in the form of HELIX.

From our perspective, the HELIX compiler transforms are an implementation of an automatic parallelization class (cyclic multithreading) that we had dismissed as less interesting than the classes from which we have garnered good results (pipelined and independent multithreading). Through the HELIX work, I am now convinced that cyclic multithreading is a worthwhile complement to pipelined and independent multithreading and a necessary component of any complete solution. This is a fundamental result that will have lasting impact on the area automatic parallelization.

Cohorts

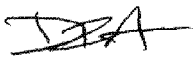
In the process of writing this letter, I have considered all of Dr. Janapa Reddi's peers at each of the top ten computer engineering research-intensive universities (a group that includes Princeton University and The University of Texas at Austin). From this group, I believe that he ranks in the top two in terms of research creativity, productivity, and impact. (Since this letter is essentially public information, I refrain from using names to be more specific.) My review of tenure decision history at these top ten institutions (based on each candidate's research record at the time of tenure review) leads me to believe that Dr. Janapa Reddi would receive tenure at any of them. Further, based on my experience on the tenure committee for Computer Science at Princeton University, I am sure that he would be granted tenure here.

Summary

Dr. Janapa Reddi has already made many impressive advancements in our field. Evidence of this is strong in the significant recognition he has already received. Given his history of identifying new areas and making real contributions of various types within them, I believe that he will continue to grow as a recognized leader in the field.

I recommend Dr. Janapa Reddi for tenure without reservation. I hope you feel as I do: this tenure case is a "no brainer". Please do not hesitate to contact me if you have any questions regarding my support for Dr. Janapa Reddi's tenure case.

Sincerely,



David I. August
Professor of Computer Science
Princeton University

Jilda Gayle

From: Bearden, Carole A <cjjp@mail.utexas.edu>
Sent: Sunday, August 7, 2016 3:52 PM
To: Tewfik, Ahmed H; jildagayle@gmail.com
Subject: Fwd: Gentle Reminder - Promotion Reference letter - Vijay Janapa Reddi
Attachments: letter.pdf; ATT00001.htm

Carole

Begin forwarded message:

> **From:** David August <august@CS.Princeton.EDU>
> **Date:** August 7, 2016 at 2:11:54 PM CDT
> **To:** "Bearden, Carole A" <cjjp@mail.utexas.edu>
> **Subject: Re: Gentle Reminder - Promotion Reference letter - Vijay Janapa Reddi**
>
> Here it is. Sorry for the delay!
>
> My website, listed in my letterhead, is http://august.princeton.edu
>
> Thanks!
>
> David
>
> On Tue, Aug 2, 2016 at 3:02 PM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:
>
> Hi Dr. August,
>
> This is a gentle reminder for the reference letter for Dr. Vijay Janapa Reddi.
>
> Many thanks,
>
> Carole
>
> **From:** Bearden, Carole A
> **Sent:** Monday, July 11, 2016 6:08 PM
> **To:** 'august@liberty-research.org' <august@liberty-research.org>
> **Cc:** Tewfik, Ahmed H (tewfik@austin.utexas.edu) <tewfik@austin.utexas.edu>; Jilda Bolton

David August

Title/Position
Professor
Degree
Ph.D., University of Illinois, Urbana/Champaign, 2000
august(@cs.princeton.edu) (609) 258-2085 221 Computer Science
Homepage
http://www.cs.princeton.edu/~august
Other Affiliations
EE

Research

Interests: Computer Architecture and Compilers.
IEEE Fellow, 2015.

Research Areas:

- Computer Architecture
- Programming Languages / Compilers

Active Research Projects:

- Liberty Research
- Structural Modeling
- THRIFT
- VELOCITY Compiler

Short Bio

David I. August joined the department as a lecturer in 1999, became an assistant professor the next year, an associate professor in 2006 and a full professor in 2012. He earned his doctoral and master's degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign. Among his professional activities, Professor August was co-program chair for MICRO 2009, and he served on the program committees for ISCA 2007, PLDI 2008, MICRO 2010, ASPLOS 2011, and Top-Picks 2012. His "Revisiting the Sequential Programming Model for the Multicore Era" was chosen for IEEE Micro's Top-Picks special issue of papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2007. He also won the Best Paper Award for "Fault-tolerant Typed Assembly Language" at the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), in June 2007. His primary research interests are in synergistic compiler and microarchitecture design.

Selected Publications

- "Parcae: A System for Flexible Parallel Execution." Arun Raman, Ayal Zaks, Jae W. Lee, and David I. August. Proceedings of the 33rd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2012.

- "Speculative Separation for Privatization and Reductions." Nick P. Johnson, Hanjun Kim, Prakash Prabhu, Ayal Zaks, and David I. August. Proceedings of the 33rd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2012.
- "A Survey of the Practice of Computational Science." Prakash Prabhu, Thomas B. Jablin, Arun Raman, Yun Zhang, Jialu Huang, Hanjun Kim, Nick P. Johnson, Feng Liu, Soumyadeep Ghosh, Stephen Beard, Taewook Oh, Matthew Zoufaly, David Walker, and David I. August. Proceedings of the 24th ACM/IEEE Conference on High Performance Computing, Networking, Storage and Analysis (SC), November 2011.
- "Automatic CPU-GPU Communication Management and Optimization." Thomas B. Jablin, Prakash Prabhu, James A. Jablin, Nick P. Johnson, Stephen R. Beard, and David I. August. Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2011.
- "Commutative Set: A Language Extension for Implicit Parallel Programming." Prakash Prabhu, Soumyadeep Ghosh, Yun Zhang, Nick P. Johnson, and David I. August. Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2011.

Georgia Tech College of Computing

BC

August 7, 2016

Professor Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
1616 Guadalupe St.
UTA 7.416
Austin, TX 78701

Re: Promotion of Prof. Vijay Janapa Reddi to rank of Associate Professor

Dear Ahmed:

I am happy to write this letter regarding the promotion of Prof. Vijay Janapa Reddi to the rank of Associate Professor at UT-Austin. What follows is based, in part, on the criteria that would be applied in a similar situation here at Georgia Tech in our School of ECE.

For some context, when Dr. Vijay Janapa Reddi graduated and was on the job market, we at Georgia Tech interviewed him in the School of Computer Science. Although he interviewed very strongly, our internal needs were not in the architecture area and thus we could not extend him an offer. However, I was quite impressed with Vijay and have kept in contact with him over the years. In this letter, I am including these interactions along with review of the materials you sent me in order to form my opinion.

I am familiar with Dr. Janapa Reddi's contributions to mobile, web-based computing. In this arena, two contributions stand out. One is his work on *GreenWeb.* This system allows for specification of QoS information at the language level in order to prioritize low energy consumption decisions in a mobile runtime. This paper was just presented at PLDI – the top conference in the compiler area. When the acceptance of the paper was announced, I had my students look into this work as I view it to be a significant, non-incremental contribution that has the potential for large impact in mobile. Related to GreenWeb is Vijay's work on *WebCore,* an architecture optimized for these same applications. This work appeared at ISCA, also a top conference, and again I had my students pay close attention to it. This was a follow-on to work on using so-called big.Little cores to optimize this application space (appearing at HPCA, again a top venue). This line of work by Vijay is both creative and has the potential for large impact in mobile applications. I can see this area he is working in as being very rich and see it continuing on into the next decade.

Dr. Janapa Reddi also works in the interface between nanotechnology implications and architectural decisions. This work began in his Ph.D. work at Harvard, and he has continued it to date. The work on characterizing power consumption in GPUs, for example, resulted in a collaboration with Tor Aamodt, one of the stand-out leaders in the GPU research space. The tool they produced from this collaboration is a useful way to measure architectural tradeoffs in GPU design and appeared at ISCA. Vijay continued with colleagues and students ini developing a second tool for capturing voltage noise in GPU architectures. This appeared in ISLPED, a top conference in the interface between architecture and electronics, and HPCA (again, a top conference in architecture). Vijay's contributions to this space are significant and, I believe, will have lasting impact over time. I see this area as being less fruitful in the long run for Vijay. If

however it is viewed instead as Vijay's interest in creating tools that aid in computer architecture research, I have a strong reason to believe he will continue making contributions in years to come.

I view the research trajectory of Dr. Janapa Reddi as consistent with a top-tier researcher in our field. He is both creative and highly productive. Other measures of research productivity are also on track. He has healthy funding from both NSF and, perhaps in our field more significant, from industry sources. As to the latter, a sign of a successful architect is one whose research matters to the point where industry is willing to cut a check to support it.

Student productivity is a critical area for us at Georgia Tech. We look to see if a candidate for tenure has demonstrated he/she can successfully advise a Ph.D. student to completion. Dr. Janapa Reddi lists two students who are on the verge of completing their degrees—a very healthy sign. He also has two additional students who have finished their M.S. and on the path to a Ph.D. Not everyone needs to build a large group of students to be a star in our field. Vijay appears to be focusing on a few students. To that end, his publication record with these students is proof this strategy is working.

In terms of his peers, I would place Dr. Janapa Reddi in the same class as Michael Taylor (UCSD-recently promoted) or Jason Mars (University of Michigan, not yet promoted). Vijay is I think more broad than Taylor and similar to Mars in research depth. Overall, in my estimate Vijay would be easily tenured at a top institution.

I summary, I strongly recommend tenuring and promoting of Dr. Vijay Janapa Reddi to the rank of Associate Professor. He would be considered worthy of the rank of Associate Professor here at Georgia Tech—or in my opinion, any department containing a top computer architecture program.

Best regards,

Thomas M. Conte
Professor, School of Computer Science, and
Professor, School of Electrical and Computer Engineering (*joint appointment*)
2015 President, IEEE Computer Society
conte@gatech.edu

Jilda Gayle

From: Tom Conte <conte@gatech.edu>
Sent: Sunday, August 7, 2016 6:54 PM
To: Tewfik, Ahmed H
Cc: Bearden, Carole A; Jilda Bolton
Subject: Re: Gentle Reminder - Promotion Reference letter - Vijay Janapa Reddi
Attachments: rec-reddi.pdf

Please see attached.

Let me know if you need any further information.

You are lucky-- You have in front of you a very easy case!

Best,
Tom

On Tue, Aug 2, 2016 at 3:19 PM, Tewfik, Ahmed H <tewfik@austin.utexas.edu> wrote:
Thanks Tom. Yes, this will work.

regards
Ahmed

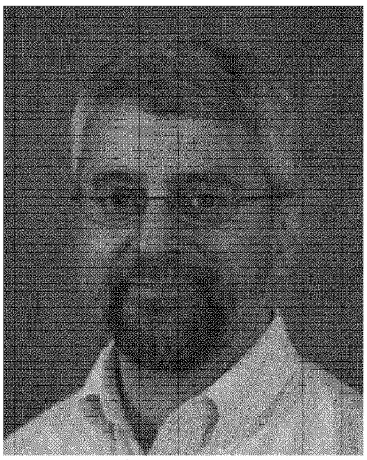
Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
1616 Guadalupe St.
UTA 7.416
Austin, TX 78701
USA

Direct: (512) 471-6179
tewfik@austin.utexas.edu

On Aug 2, 2016, at 9:11 PM, Tom Conte <conte@gatech.edu> wrote:

> Thank you and sorry I am so late.
> I need this weekend to finish it.
> Is that acceptable?
>
> On Tue, Aug 2, 2016 at 2:55 PM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:
>
> Dr. Conte,

Thomas Conte



Thomas Conte
Professor, Joint with the School of Electrical and Computer Engineering
Email:
conte@cc.gatech.edu
Personal webpage:
http://www.cc.gatech.edu/~conte

Biography:
Tom Conte holds a joint appointment in the Schools of Computer Science and Electrical & Computer Engineering at the Georgia Institute of Technology. His research is in the areas of computer architecture and compiler optimization, with emphasis on manycore architectures, microprocessor architectures, back-end compiler code generation, architectural performance evaluation and embedded computer system architectures.

Dr. Conte was the 2015 President of the IEEE Computer Society, and also a fellow of the IEEE. Since 2011, he has co-led the IEEE Rebooting Computing Initiative.

C

PENNSTATE

Department of Computer Science and Engineering

College of Engineering

The Pennsylvania State University
111 Information Sciences and Technology Building
University Park, PA 16802

814-865-9505

Fax: 814-865-3176

July 31, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
University of Texas at Austin
1616 Guadalupe St.
UTA Building, 7th Floor
Austin, Texas 78701

Dear Professor Tewfik:

I am pleased to write this letter of evaluation for Dr. Vijay Janapa Reddi, who is being considered for tenure and promotion to the rank of an Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. My evaluation is based on his curriculum vitae, my familiarity with his research work over the last several years and the selected publications that were sent to me. I have read and reviewed a number of his papers and have met him at several conferences. I hold his work in very high regard.

Vijay is internationally known for his research accomplishments in the broad area of computer architecture. In particular, his research spans from low-level hardware (circuit/microarchitecture) design to system software (compiler and OS) and to application-level for designing energy-efficient, high performance computing systems as well as handheld/mobile systems. Although he has made several fundamental contributions in these areas, I will highlight a couple of his most recent influential works in this letter. First, Vijay is a pioneer in the area of designing energy-efficient mobile architectures. Today's mobile devices have grown in sophistication to run a wide variety of applications that require real-time processing of large volumes of data. Supporting such applications within the stringent power budgets of a handheld, while satisfying the application-level QoS requirements, is a challenging task. Vijay has published a series of papers in this area – understanding the role of CPUs for mobile web browsing (Micro2015, HPCA2016), proposing the Webcore microarchitecture specialized for running Web application (ISCA2014), developing a Web language extension framework (GreenWeb) for expressing users' quality of experience (QoE) Characteristics (PLDI2016), and designing a runtime framework for energy-efficient execution of Web applications on specialized hardware (HPCA-15). His group has designed a working prototype using Google Chrome to demonstrate the energy-efficiency of his proposed ideas. Another of Vijay's major works is the proposal to use power-efficient small (wimpy) cores for designing large datacenters/cloud platforms. Unlike the traditional approach of using power hungry server cores, he demonstrated that the wimpy core approach for designing datacenters could provide up to 5x energy-efficiency (ISCA2010). This wimpy core concept has been adopted in several commercial datacenter designs. His other piece of work that has been well cited is GPUWattch (ISCA2013), which is an open-source tool for modeling power consumption in GPU microarchitecture.

Vijay's publication record is a testimony to his research accomplishments. He has published forty conference and journal papers, ten workshop papers and two synthesis lecture manuscripts in the above areas. Most of his research results have appeared in highly selective international conference proceedings such as ISCA, MICRO, HPCA, PLDI, and ISLPED, and ICCD, and top-tier international journals such as the ACM Trans. on Computer Systems (TACO). He has received several awards including two best paper awards and three papers have been accepted in MICRO Top Picks. In summary, his research record is simply outstanding and I expect significant contributions from him in these evolving areas.

Other factors that support one's research credentials are graduate student supervision and external funding. Vijay has supervised two Ph.D. students, two MS Students and is currently advising two Ph.D. students and two MS students. In addition, he has strong research collaboration with several groups in academia and industry. His research has been funded by four NSF grants, a grant from SRC, and industry funding from Google, Intel and AMD. This certainly speaks about the strength and breadth of his research and its practical relevance.

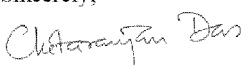
While I don't have any firsthand knowledge of Vijay's classroom teaching ability, I have listened to a couple of his conference presentations. He is a very good speaker with the ability to abstract the essential elements of a topic, and thus, a listener gets a good understanding of the context as well as details. His Vitae shows that he has taught a freshman embedded systems course and two graduate compiler courses at Austin and has received very good evaluations. Moreover, he is deeply involved in teaching hands-on computer science to 5th and 6th grade students in Austin and improving the classroom teaching environment with wearable devices. This clearly demonstrates his seriousness towards teaching.

Vijay is also quite active in various professional society activities. He has served as the Program Chair for CGO, and will serve as the General Chair for CGO-2017. In addition, he has served as a Program Committee Member and Session Chair for many international conferences such as ISCA, HPCA, MICRO and PACT. Also, he has been a very good citizen of the community by serving as a referee for many journals and conferences. His service to the department is also impressive.

In conclusion, I strongly believe that Vijay's scholarly contribution is outstanding and I would rank him as one of the best researchers among his peers. Because of his extraordinary research accomplishments, he won the IEEE Computer Society's Young Computer Architect Award in 2016. This is an annual award given to the best young computer architect. I have been on our department Promotion and Tenure Committee and have written many promotion letters for research-intensive schools. Based on my experience, I can certainly say that Vijay would have no problem in getting promotion and tenure at Penn State and for that matter in any major school. I very enthusiastically support his tenure and promotion to the rank of an Associate Professor.

If you need any additional information, please do not hesitate to contact me.

Sincerely,



Chita R. Das
Distinguished Professor and Interim Head of Computer Science and Engineering
Pennsylvania State University

Jilda Gayle

From: Tewfik, Ahmed H <tewfik@austin.utexas.edu>
Sent: Friday, August 5, 2016 4:19 PM
To: jildagayle@gmail.com
Subject: Fwd: Reference letter for Dr. Reddi
Attachments: vijayreddi-letter.doc; Untitled attachment 00477.htm
Signed By: tewfik@austin.utexas.edu

regards
Ahmed

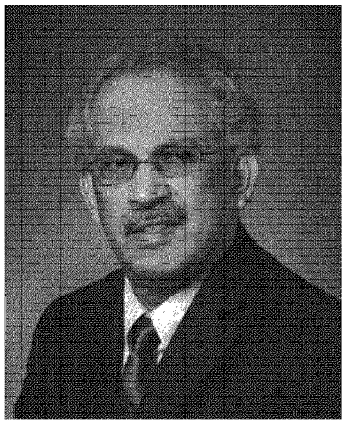
Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
The University of Texas at Austin
1616 Guadalupe St.
UTA 7.416
Austin, TX 78701
USA

Direct: (512) 471-6179
tewfik@austin.utexas.edu

Begin forwarded message:

> **Resent-From:** <tewfik@austin.utexas.edu>
> **From:** Chita Das <chitadas@gmail.com>
> **Date:** August 5, 2016 at 11:53:07 PM GMT+3
> **To:** <tewfik@austin.utexas.edu>, <cjjp@mail.utexas.edu>, Chita Das <chitadas@gmail.com>
> **Subject: Reference letter for Dr. Reddi**
>
> Dear Prof. Tewfik,
>
> Enclosed please find my reference letter for Vijay.
>
> Please let me know if you need any other info.
>
> Thanks,
> --Chita

Chita R. Das



Distinguished Professor
Interim Head
Department of Computer Science and Engineering
Penn State University

354F IST Building
University Park, PA, 16802

Google Scholar Profile
High Performance Computing Lab

RECENT NEWS

- Paper accepted in HPCA 2017.
- Paper accepted in MICRO 2016.
- 2 Papers accepted in PACT 2016.

BRIEF BIO

Chita Das is a Distinguished Professor of Computer Science and Engineering at the Pennsylvania State University. His main areas of interest include parallel and distributed computer architectures, multi-core architectures, mobile computing, performance evaluation, and fault-tolerant computing. In particular, he has worked extensively in the area of design and analysis of interconnection networks/on-chip interconnects. He has published more than 200 papers in the above areas, has served on many program committees, and editorial boards.

RESEARCH INTERESTS

Parallel & Distributed Computer Architectures; Multi-core/SoC Architectures; GPGPU systems; Heterogeneous Architectures; Communication Networks & Communication Mechanisms; Network-on-Chips Architectures; Resource Management

(Scheduling); QoS support in Clusters and Internet; Performance Evaluation; Fault-tolerant Computing; Mobile Platforms.

PUBLICATIONS

Click here for the list of publications.

STUDENTS

This list contains the list of all my current and past PhD students.

C

STANFORD ELECTRICAL ENGINEERING

Christos Kozyrakis
Associate Professor
Department of Electrical Engineering
Department of Computer Science

Gates Hall Room 304
353 Serra Mall
Stanford University
Stanford, CA 94305-9030

Friday, August 12, 2016

To: Professor Ahmed Tewfik
Department of Electrical and Computer Engineering
Cockrell School of Engineering
University of Texas at Austin

Subject: Promotion recommendation for Dr. Janapa Reddi

Dear Professor Tewfik,

It is a great pleasure to strongly recommend Dr. Vinay Janapa Reddi for promotion to the rank of Associate Professor with indefinite tenure at the University of Texas at Austin. Dr. Janapa Reddi is one of the leading experts in the intersection of computer architecture and runtime management systems. Throughout his career, he has led or participated in influential research projects that produced significant technical results and widely-used research tools. He has excelled under any metric that measures impact in his area of expertise and clearly deserves this promotion.

To establish my credentials for this recommendation, I have attached a short biographical note at the end of this letter. As my research interests overlap with those of Dr. Janapa Reddi in the areas of datacenter computing and high-speed simulation, I have followed his work closely over the years. I have also used in my research some of the tools he developed. Overall, I am quite familiar with his accomplishments thus far, his technical skills, and his future potential as an academic researcher.

Dr. Janapa Reddi's research at UT Austin concentrated on energy-efficient platforms for mobile systems and exascale systems. I am particularly impressed with his work on high-performance, energy-efficient, mobile web computing. First, his work targeted an important problem, the scalability of the ubiquitous mobile devices. Surprisingly, this challenge is comparatively overlooked by computer architects that find it easier to focus on traditional server platforms. Second, Dr. Janapa Reddi and his team focused on a key opportunity: knowledge of what constitutes a good quality-of-experience (QoE) for mobile applications allows us to build platforms that dynamically right-size their performance and energy consumption to the actual user needs at the time. Third, they built a comprehensive platform to exploit this opportunity. The platform includes GreenWeb, a language extension to popular Web languages (CSS, JavaScript, etc.) that allows programmers define QoE requirements; Wert, a browser runtime that dynamically tunes the types and settings of processing cores in order to meet QoE requirements at lowest energy consumption; WebCore, a processor architecture that is specialized to accelerate and reduce power consumption for critical aspects of mobile computing like style resolution. The results of all three aspects of the project are impressive and I am certain they will strongly influence the direction of mobile Web platforms and mobile architectures in the near future. This is exactly the kind of thought-provoking and vertical project that we should encourage any young faculty to undertake.

Dr. Janapa Reddi has also produced important results in the area of large-scale systems. His paper on datacenter computing with low-power cores sparked one of the most interesting debates in the computer architecture community in the last few years. His proposals on voltage and reliability management on multi-core chips and graphics processors are considered state-of-the-art.

Phone: (650) 725-3716 • Fax: (650) 725-6949 • E-mail: christos@cc.stanford.edu • Web: http://csl.stanford.edu/~christos

Moreover, Dr. Janapa Reddi has made significant contributions through his work on simulation and instrumentation tools. He was a major contributor to the Pin project, a tool for dynamic binary instrumentation. Pin has been widely used by numerous researchers for projects across all areas of computer architecture and programming systems. I have personally used Pin in two projects in order to build a low-overhead security system and as the basis of a highly parallel architecture simulator. Dr. Janapa Reddi is also a major contributor in the recently released Simulation Analysis Engine (SAE), a platform for full-system instrumentation for software analysis and architectural exploration. I expect SAE will have similar impact as Pin.

Dr. Janapa Reddi is broadly recognized as one of the leading researchers in his generation. He recently received the IEEE TCCA Young Computer Architect Award that recognizes an individual that has made outstanding, innovative research contributions to computer architecture within the first 6 years after completing his/her PhD degree. This award also establishes how he compares to his peers. His research has been recognized with several awards, including 3 Top Picks in Computer Architecture, the PLDI Most Influential Paper Award, and several best paper awards. He has an extensive publication record in top conferences in computer architecture and programming languages (ISCA, ASPLOS, MICRO, PLDI, CGO, DAC, etc.). There are not many researchers that can perform high caliber research at the intersection of two fields and can publish at top venues in both areas. Dr. Janapa Reddi's papers consistently showcase a well-planned line of research with systematic consideration of all aspects of a problem.

Overall, Dr. Janapa Reddi has exceeded all my expectations for a solid, young researcher in computer architecture and runtime systems. I am certain he will perform equally well, if not better, as a mid-career and senior colleague, and that he will be one of the leader of our field.

Don't hesitate to contact me for any further information.

Sincerely,

Christos Kozyrakis
Stanford University

Biographical note: Christos Kozyrakis is an Associate Professor of Electrical Engineering & Computer Science at Stanford University and a Professor of Computer and Communication Sciences at EPFL. He received a BS degree from the University of Crete (Greece) and a PhD degree from the University of California at Berkeley (USA), both in Computer Science. He is a fellow of the IEEE and a senior member of the ACM. He has received the ACM SIGARCH Maurice Wilkes award, the NSF Career Award, an IBM Faculty Award, the Okawa Foundation Research Grant, the Noyce Family Faculty Scholarship, and the Willard R. and Inez Kerr Bell Faculty Scholarship.

Dr. Kozyrakis works on architectures, runtime environments, and programming models for parallel computer systems. At Berkeley, he developed the IRAM architecture, a novel media-processor system that combined vector processing with embedded DRAM technology. At Stanford, he led the Transactional Coherence and Consistency (TCC) project at Stanford that developed hardware and software mechanisms for programming with transactional memory. He also led the Daksha project, that developed practical hardware support and security policies to deter high-level and low-level security attacks against deployed software. Dr. Kozyrakis is currently working on resource efficient computing for warehouse-scale datacenters.

For further information, please refer to http://csl.stanford.edu/~christos.

Phone: (650) 725-3716 • Fax: (650) 725-6949 • E-mail: christos@cc.stanford.edu • Web: http://csl.stanford.edu/~christos

Jilda Gayle

From: Kozyrakis Christos <christos.kozyrakis@epfl.ch>
Sent: Saturday, August 13, 2016 3:21 AM
To: Bearden, Carole A
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: Gentle reminder - Promotion Reference letter - Vijay Janapa Reddi
Attachments: reddi.tenure.2016.pdf; ATT00001.htm

Dear Ahmed and Carole,
please find attached my reference letter for Dr. Janapa Reddi.
Regards

On Aug 1, 2016, at 9:15 PM, Bearden, Carole A <cjjp@mail.utexas.edu> wrote:

Dr. Kozyrakis,

This is a gentle reminder requesting the promotions letter for Dr. Vijay Janapa Reddi.

Best regards,

Carole

From: Bearden, Carole A
Sent: Friday, June 24, 2016 11:48 AM
To: 'christos@ee.stanford.edu' <christos@ee.stanford.edu>; 'christos.kozyrakis@epfl.ch' <christos.kozyrakis@epfl.ch>
Cc: Tewfik, Ahmed H (tewfik@austin.utexas.edu) <tewfik@austin.utexas.edu>; Jilda Bolton (jildagayle@gmail.com) <jildagayle@gmail.com>
Subject: Promotion Reference letter - Vijay Janapa Reddi

Dr. Kozyrakis,

Thank you for agreeing to write a promotion reference letter for Dr. Vijay Janapa Reddi **by July 25, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Janapa Reddi posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

Carole Bearden
Executive Assistant
Electrical and Computer Engineering
The University of Texas at Austin
(512) 471-4540

What starts here changes the world

UNIVERSITY OF MICHIGAN
Advanced Computer Architecture Laboratory
COMPUTER SCIENCE & ENGINEERING

2260 Hayward Ave.
Ann Arbor, MI 48109-2121
PH: 734 936-1602 FAX: 734 763-4617

C

July 21, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
University of Texas at Austin
1616 Guadalupe St.
Austin, TX 78701

Dear Prof. Tewfik,

It gives me great pleasure to express my enthusiastic support for the promotion case of Prof. Vijay Janapa Reddi to the level of Associate Professor with tenure in your department. I have known him for the past ten years since he was a Masters student at the University of Colorado. I regularly interact with him at technical conferences and worked closely with him as the co-chair for a conference in 2014-15. I have had ample time to observe him as a student and then as a faculty member, thus I believe that I can provide a thorough evaluation of his career to this point and his potential going forward.

In this letter, I will first highlight his biggest research contributions and assess their impact on the field, followed by discussing his teaching/mentoring and service contributions, and finally conclude with a summary of my recommendation.

Research contributions: Prof. Reddi is an outstanding researcher and respected scholar in the areas of computer architecture and compiler code generation. One of his best strengths is his ability to push the boundaries of research to define and develop truly innovative solutions to difficult problems. I am very impressed by his work on pushing energy efficiency into the Web domain which has generally been disregarded by the computer architecture community because of its opaqueness, complexity, and difficulty to reason about. Prof. Reddi's group overcame these difficulties to jump in and attack the problem of energy efficiency for mobile Web browsers. He showed that simple analysis of a webpage structure (top-level components, CSS style file, etc.) is both light weight and can yield large amounts of information about the characteristics of the computation required to render the page. This information is fed back to the operating system to manage heterogeneous hardware, such as the use of a big/little cores or setting of dynamic voltage/frequency levels. The work yields significant gains for many popular websites on real-world hardware. The work has been so successful that a version of the technology is being integrated into Samsung's Tizen OS. Such technology transfer is rare for any academic researcher and is a real testimonial to both the importance and high practical value of the work. This thrust of his research has an impressive list of top-tier publications including three HPCA (2013, 2015 and 16) and one ISCA (2014) papers attesting to quality and breadth of the work.

Despite his relatively short career, Prof. Reddi has already had a profound impact creating tools that are seamlessly used by students, faculty, and engineers in the computer systems community. He helped create PIN, one of the most ubiquitous tools in both research and the classroom with hundreds of thousands of downloads. There are few tools developed in the compiler and computer architecture communities that achieve this status, thus this is quite an achievement. To recognize the importance of the work, his 2005 PLDI paper was awarded the *2015 SIGPLAN Most Influential Paper Award*. Now, one could fairly ask, Prof. Reddi was the eighth of nine

authors, how much did he really contribute? His largest contribution was transforming PIN from an internal Intel tool to a general-purpose instrumentation tool for the entire community. He led the creation of an extensive set of PIN tutorials at the leading computer architecture conferences, demonstrated the use cases of how PIN could enable new forms of research, and created the material to allow people to adopt and be productive with PIN. Transforming a tool for experts into one for the masses is a huge undertaking that requires substantial effort, and he made it look easy. While I have emphasized the usability and publicity of the tool, he also contributed heavily to the early technical design and development of PIN. As evidence to this claim, he was the first author of the original workshop paper that preceded the famous PLDI paper presented at the *7th International Workshop on Computer Architecture Education* in 2014.

Prof. Reddi has followed up Pin with another tool that is rapidly gaining popularity called GPUWattch. This tool computes energy consumption data within the popular GP-GPUSim simulator that is used in nearly every research paper that examines GPU scheduling, microarchitecture, and memory system design. The development of GPUWattch was both timely and well executed, truly raising the bar on graphics processing research in the computer architecture community to treat energy as a first-class design constraint. Tools can have a profound impact on the community both in terms of how it does research and what research topics are investigated, and Prof. Reddi has demonstrated two strong successes in his career to date.

Teaching & Mentoring: While I have never seen Prof. Reddi teach a class in person, he has an impressive teaching record at Texas. It is evident that he cares deeply about the students and this comes across in his lectures and one-on-one interactions. He is also a gifted presenter who does a great job of combining principle with practice so that the students understand why they are learning something and where it is used in the real world. As a graduate student mentor, he is outstanding and behaves more like a seasoned professional than an Assistant Professor. I have directly observed him mentor one of his students, Yuhao Zhu, as a member of his PhD dissertation committee. He provides a great combination of creative directions to investigate, guidance to get the students past sticking points, and encouragement and motivation when the work gets challenging. He knows how to ask the right questions to get students to think more deeply about their work and identify potential flaws. And, he genuinely cares about his students being successful, and this is clearly evident to them which make them more eager to listen to his suggestions and feedback. Overall, I am confident that Prof. Reddi would rank among our top instructors and mentors in my own department.

Service Contributions: His excellence is also pervasive in his service to the broader computer architecture and compiler communities. I had the opportunity to work directly with him as Program Co-Chairs for the *2015 International Symposium on Code Generation and Optimization*. It was a pleasure to work with him. He was consistently prepared with informed ideas and methods to handle the program chair duties. He took strong initiative to manage the selection of the program committee, distribute the papers, and manage reviews. But at the same time, he welcomed my input to the process, thus it was the perfect balance. It was an honor to work with him, and I would not hesitate in the slightest to do so again in the future. He is currently serving as the General Chair for the *2017 International Symposium on Code Generation and Optimization* that will be held in Austin and doing a great job from everything that I have heard.

Conclusion – Creative, technically excellent and well executed research is rarely an isolated occurrence. Rather, special individuals produce consistently strong research across their careers, which is the case with Prof. Reddi. Looking across his career, three Top Picks is computer architecture, Best Paper Awards at MICRO and HPCA, a PLDI Most Influential Paper Award, an Intel Early Career Award, and most recently the 2016 IEEE TCCA Young Computer Architect Award testify to his strong level of technical excellence. He already has had a strong impact on

the computer architecture community through the creation of two ubiquitous tools and the transfer of his Web work to a Samsung product. He has a keen mind for identifying both the right problems to work on as well as developing practical solutions that can be deployed in the real-world. Unlike most Assistant Professors, he is trend setter rather than a follower.

I am confident that he would be promoted in my department at the University of Michigan as his combined research, teaching, and service records are outstanding. In comparison to faculty members in his cohort, he stacks up very well to the very best in his group. His cross domain expertise in computer architecture and compiler code generation really sets him apart as his technical breadth is matched by few in the community. He is clearly over the bar for promotion and tenure, and I strongly urge you to do your best to keep him at Texas as he has an outstanding career ahead of him.

Sincerely,

Scott A. Mahlke
Professor and Associate Chair
Electrical Engineering and Computer Science Department
University of Michigan
Email: mahlke@umich.edu
Tel: (734) 936-1602

Summary Vita – Scott Mahlke is a Professor and the Associate Chair in the EECS Department at the University of Michigan. He joined Michigan in 2001 after spending 6 years at Hewlett Packard Laboratories as a Senior Researcher. He got his Ph.D. in Electrical Engineering from the University of Illinois at Urbana-Champaign in 1997. His area of research is computer architecture and compilers, with specialization in customized processing systems, reliability, and compiler code generation, where he has published more than 200 papers. He leads the Compilers Creating Custom Processors research group with funding from ARM Ltd., Intel, Samsung, Huawei, Department of Energy, and the National Science Foundation. To date, 22 Ph.D. students have graduated from his group and are now employed at variety of leading technology companies including Google, Facebook, Intel, AMD, Oracle, Qualcomm, ARM, and Synopsys.

Jilda Gayle

From: scott.mahlke@gmail.com on behalf of Scott Mahlke <mahlke@umich.edu>
Sent: Friday, July 22, 2016 3:45 PM
To: Jilda Gayle
Cc: Tewfik, Ahmed H; Bearden, Carole A
Subject: Re: Promotion Reference letter - Vijay Janapa Reddi
Attachments: VijayReddiJul16signed.pdf

Jilda,

Sure, here is a signed/scanned version of the letter.

Regards,
Scott

On Fri, Jul 22, 2016 at 9:58 AM, Jilda Gayle <jildagayle@gmail.com> wrote:

Hi Dr. Mahlke,

Actually we do need signed letters but an electronic signature on your letter will be just fine.

Thank you!

Jilda

From: scott.mahlke@gmail.com [mailto:scott.mahlke@gmail.com] **On Behalf Of** Scott Mahlke
Sent: Thursday, July 21, 2016 3:06 PM
To: Bearden, Carole A <cjjp@mail.utexas.edu>
Cc: Tewfik, Ahmed H <tewfik@austin.utexas.edu>; Jilda Bolton (jildagayle@gmail.com) <jildagayle@gmail.com>
Subject: Re: Promotion Reference letter - Vijay Janapa Reddi

Ahmed, Carole,

Please find attached my evaluation letter for Prof. Reddi's promotion case. If you need a scanned/signed version, please let me know and I can get that to you.

Regards,

Scott

BC

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Professor Onur Mutlu
Department of Computer Science
ETH Zürich
CAB F 74.2
Universitätstrasse 6
8092 Zürich
Switzerland

Phone +41 44 632 88 53
Fax +41 44 632 10 59
onur.mutlu@inf.ethz.ch
https://users.ece.cmu.edu/~omutlu/

August 21, 2016

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering

Dear Professor Tewfik:

I am writing this letter in response to your request for my assessment of Dr. Vijay Janapa Reddi's scholarly contributions with respect to his tenure and advancement to the rank of Associate Professor at the University of Texas at Austin. I have known Dr. Janapa Reddi for almost ten years, since when he was a graduate student at Harvard University and followed his research since then. Although I never worked with him, I interacted with him on many occasions in person and intended to hire him as an intern to the Computer Architecture Group while I was at Microsoft Research. On a more personal note, I have always enjoyed my technical interactions with him and found them stimulating.

Dr. Janapa Reddi became an established researcher who has amassed a significant amount of high-quality work in computer architecture with significant and growing impact. He has distinguished himself as a leader who has expanded the field of computer architecture in new directions by making outstanding and leading contributions to mobile computer architectures and resilient computer architectures. I therefore enthusiastically support Dr. Vijay Janapa Reddi's tenure and promotion to Associate Professor.

Dr. Janapa Reddi is highly regarded as a leader in two innovative areas in the computer architecture community: 1) mobile architectures, with a focus on solid experimental analysis and new customized system designs for them, and 2) resilient architectures, with a major focus on voltage noise. He has produced consistently outstanding and prolific research in both areas, and has written high-quality papers on both topics. To keep this letter concise, I will give a few examples from these two major areas where Dr. Janapa Reddi distinguished himself as a leading researcher. I will also briefly touch upon a third area where he made very high-impact contributions on, which is the development and release of widely-used research infrastructures and tools, including the Pin dynamic binary instrumentation tool (PLDI 2005) and the GPUWattch energy and power modeling tool (ISCA 2013).

First, a comment on Dr. Janapa Reddi's experimental approach and rigor. I find Vijay's approach to research to be very solid and thorough, which is reflected in the experimental rigor of his papers. He performs very thorough experimental characterizations of real systems and drives his creative solutions based on the results of such characterizations. For example, his work has provided invaluable experimental analyses and data, the first of their kind, of voltage noise in modern processors (MICRO 2010), voltage noise in GPU systems (MICRO 2015), energy, performance and QoS effects of using mobile cores in server systems (ISCA 2010), and experimental analysis of Web Browsing and its bottlenecks in mobile systems (HPCA 2013, ISCA 2014, HPCA 2016). I regularly recommend these works to anyone interested in getting a clear understanding of real system characterization of the respective topics. Vijay's clear track record in producing such invaluable experimental analyses is relatively unique, has already had significant impact and will likely continue to grow in its impact given the importance and industrial relevance of the subject areas.

Mobile architectures. Dr. Janapa Reddi has pioneered the computer architecture research on customized cores for mobile systems, e.g., cell phones, for high energy efficiency, with a focus on Web Browsing. He has a string of very well-written top conference contributions in this area, including his papers at HPCA 2013, ISCA 2014, HPCA 2015, HPCA 2016, and PLDI 2016 (and likely more I am not as familiar with).

I will first point out one earlier and high-impact contribution, which I believe led to his later work in custom core designs for mobile systems. Vijay was the first to experimentally evaluate the use of small versus big cores for server systems for Web Search, and demonstrate the benefits and downsides of each. In his ISCA 2010 paper, "Web Search using Mobile Cores: Quantifying and Mitigating the Price of Efficiency," he thoroughly analyzed the performance, power consumption and quality of service (QoS) effects of mobile cores on Microsoft's Bing server workload. This work demonstrated, with solid experimental analysis, for the first time that using mobile cores can significantly improve energy efficiency in such server workloads yet doing so also degrades QoS and latency for especially complex web search queries. It argued for mitigating shortcomings of mobile cores in multiple ways, including with more heterogeneous designs. This work was seminal because it provided the first experimental answer to a critical question with a solid and thorough analysis: "What type of cores should server systems use?" Later influential works in the computer architecture community that, years later, aimed to devise specialized architectures for server systems were heavily influenced by this work and in fact repeated many of the findings in Vijay's ISCA 2010 work.

Two of Dr. Janapa Reddi's later works, one in HPCA 2013 and the sequel in ISCA 2014, established the standard in analysis of Web Browsing on modern hardware and developed custom hardware for Web Browsing, called WebCore. Web Browsing is critically important since that is how mobile users spend much of their time and the energy of their mobile devices. Vijay had the foresight to tackle bottlenecks in mobile web browsers. His HPCA 2013 paper is the first one, to my knowledge, to analyze web browser performance and energy by analyzing the execution of 5000 webpages on multiple types of cores and breaking down execution to different components of webpage loading. This work identified and demonstrated the heterogeneity in the performance demands of both different webpages and different components of the webpages, developed a model to predict webpage rendering performance and energy efficiency on various cores, and introduced a new webpage-aware workload scheduler design that decides what type of core, big versus small, the webpage should be rendered on. It showed significant energy savings with this new webpage-aware core scheduler design. I find this work very forward looking and refreshing, done at a time when very few people were even thinking about mobile system efficiency in academia, and can easily see mobile system software taking advantage of the techniques Vijay proposed in it.

Building on the insights from his earlier webpage browsing analyses on big and small cores, Dr, Janapa Reddi later developed the idea of WebCore (ISCA 2014), a customized core that has hardware acceleration mechanisms to render Web content. The acceleration mechanisms target the heaviest kernels limiting Web rendering performance based on a rigorous experimental analysis of various kernels' web rendering performance and energy consumption. Given that Web Browsers are so widely used in mobile systems and in any ways the main application in such systems, having such hardware acceleration support for web browsing that greatly improves energy efficiency can be adopted by industry and have very high impact on the design of current and future mobile systems-on-chip. Vijay's work is in this regard very forward looking, unique in academia, and a joy to follow. Vijay has clearly led top-notch work in this area and set the state-of-the-art.

Dr. Janapa Reddi, together with his graduate students, has done many other works on Web-specific system design, spanning programming languages (e.g., GreenWeb, PLDI 2016, being a prime example where he provides pragmas such that the programmers can provide quality of experience requirements for systems to satisfy), hardware architectures, and system software runtimes. For brevity, I will omit the discussion of these works, but suffice it to say that Vijay comprehensively pushes forward the state of the art at multiple layers of the computing stack, with significant insight and novel ground covered in each of his informative and joyful-to-read works.

Resilient architectures: Voltage noise and its mitigation. Dr. Janapa Reddi is without a doubt the leading expert and pioneer in voltage noise characterization and mitigation in modern general purpose processors and Graphics Processing Units (GPUs). He has done seminal work in this area, which deservedly received multiple awards (including one HPCA 2009 Best Paper Award and IEEE Micro Top Picks paper selection for his MICRO 2010 paper, both of which I am intimately familiar with, as I mention below).

This is a critically important research topic, as the noise induced by voltage fluctuations (voltage noise) in smaller-scale technology nodes tends to set the limit of how low voltage can be reliably reduced in modern systems. Voltage reduction is critical for energy savings and technology scaling, yet as voltage is reduced, the noise in voltage becomes a bigger problem, sometimes preventing the further scaling of voltage due to voltage-noise-induced failures. To avoid this, manufacturers usually add a large margin, or guardband, to the voltage level, which leads to significant loss in energy efficiency. Thus, understanding the characteristics of voltage noise and devising mechanisms to mitigate such noise would allow hardware designers to build much more resilient and energy efficient systems that can reduce the voltage margins. Vijay was and continues to be a pioneer in doing exactly that: building such an understanding and developing mechanisms to tolerate voltage noise.

In a series of papers during his doctoral work, Dr. Janapa Reddi provided the first characterization of voltage induced noise in a modern microprocessor (MICRO 2010; selected as a Top Pick by IEEE Micro) and introduced methods for predicting voltage emergencies via signatures of microarchitectural events and mitigating them (HPCA 2009 Best Paper Award).

These are seminal works on voltage with invaluable data on a modern system's voltage behavior, which I assign my students to study. Vijay's collective doctoral work developed seminal approaches to predicting and mitigating voltage noise emergencies using hardware and software. I will not belabor on these, although these do attest to the quality of work Vijay has been producing since his graduate school days. They are very clear papers with many insights.

Vijay did not stop there in this line of research. He has recently been doing leading work on the characterization and mitigation of voltage noise in GPUs in another series of insightful papers (ISLPED 2014, HPCA 2015, MICRO 2015). His MICRO 2015 work provides a solid characterization of the voltage margins in modern GPUs via experimental data, showing significant opportunity for energy reduction. It develops techniques for predicting the minimum reliable voltage to operate a particular workload at. This paper is the first one to not only experimentally characterize GPU voltage margins in real systems but also show that minimum operating voltage is strongly dependent on program behavior and can be predicted via monitoring of the performance counters. I very much like this work because I believe the experimental data and the new insight into program-dependent minimum voltage behavior will pave the way to many future works that can develop cross-layer mechanisms for improving GPU energy efficiency and resilience.

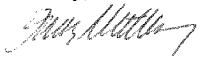
Research infrastructures and tools. A great strength of Dr. Janapa Reddi is his contribution to open-source tools that are very widely used by the computer architecture community. He is an avid tool developer and enabler of the use of such tools by the larger community. As an intern at Intel, he co-developed the Pin binary instrumentation tool, which is a customizable program analysis tool that is in widespread use for both research and teaching. In fact, Vijay is the first author on the first publication related to Pin, which appeared in the Workshop on Computer Architecture Education in June 2004, with the title "PIN: A Binary Instrumentation Tool in Computer Architecture Research and Education." He helped transform the tool for widespread use by the research community by both maintaining and enhancing the tool and developing and delivering tutorials in leading computer architecture conferences over the years. This is a tool that has enabled significant research and I think Vijay is responsible for not only co-developing it but also doing the hard work to enable its adoption in the field by most involved in computer architecture research and education.

More recently, Vijay developed and released the first energy modeling infrastructure for GPU architectures, GPUWattch. This tool fills a huge gap in GPU architecture evaluation. We have used this tool in my group's GPU architecture research and found it to be greatly valuable and effective in modeling energy of GPGPU systems. I believe this tool has become the de facto standard tool to evaluate GPU energy and power consumption in modern systems and is a strong attestation to Vijay's skills as a researcher who can lead the field with not only creative and forward looking ideas but also extremely useful, practical and timely tools.

Recognition and Leadership. I will not go into the detail of the awards Dr. Janapa Reddi received, except I will relate a few of these I am very much familiar with. First, I was on the awards committee when Vijay received the IEEE Computer Society Young Computer Architect Award this year (in 2016). He was easily the top candidate among a set of strong ones and the committee had an easy time deciding to give the award to him. He was awarded due to his forward looking and outstanding research contributions in mobile computing and resilient architectures. Second, I was the selection committee co-chair when his MICRO 2010 paper got selected as an IEEE Micro Top Pick. It was an easy choice for the committee to take it in as the first comprehensive study for voltage noise that was very thorough. Third, Vijay presented his paper in the Best Paper Session at HPCA 2009, which I attended (and in fact our paper was presented in the same session). He delivered an outstanding and extremely clear presentation, as he always has done when I saw him give talks. He well deservedly received the Best Paper Award in HPCA 2009 for his voltage emergency prediction work. I believe he will continue to receive many other such awards and lead the field with his solid research.

In summary, I think very highly of Dr. Vijay Janapa Reddi's research and credentials as a junior professor. He is without a doubt a leading researcher who is blazing the trail in mobile computer architectures and resilient computer architectures, with high impact and technically solid research. He is clearly a leading researcher among his peers. His work has already had significant impact, which I believe will only continue to grow due to the importance and relevance of the subject matter he chooses and the invaluableness of the experimental data and tools he exposes to the broader community. I strongly believe Dr. Vijay Janapa Reddi is exceptionally qualified for promotion to Associate Professor at the University of Texas at Austin and therefore enthusiastically support his tenure and promotion to Associate Professor.

Sincerely,



Onur Mutlu
Full Professor, ETH Zürich
Adjunct Professor, Carnegie Mellon University
onur.mutlu@inf.ethz.ch
https://users.ece.cmu.edu/~omutlu/

Jilda Gayle

From: Mutlu Onur <onur.mutlu@inf.ethz.ch>
Sent: Sunday, August 21, 2016 9:24 AM
To: Bearden, Carole A; Mutlu Onur
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: Gentle reminder - Promotion Reference letter - Vijay Janapa Reddi
Attachments: vijay-janapa-reddi-tenure-letter-august-20-2016-eth.pdf; onurmutlu-CV-jun-27-2016-v2.pdf

Dear Ahmed and Carole,

I attached my letter for Dr. Vijay Janapa Reddi.

My CV is also attached (~2 months old).

Onur

From: "Bearden, Carole A" <cjjp@mail.utexas.edu>
Date: Tuesday, August 16, 2016 at 5:38 AM
To: Mutlu Onur <onur.mutlu@inf.ethz.ch>
Cc: "Tewfik, Ahmed H" <tewfik@austin.utexas.edu>, "Jilda Bolton (jildagayle@gmail.com)" <jildagayle@gmail.com>
Subject: RE: Gentle reminder - Promotion Reference letter - Vijay Janapa Reddi

Onur,

I just want to remind you that your letter has to be turned in before or on the 20th. We cannot use your letter if it is late and it will look bad for Vijay's promotion.

Best,

Carole

From: Bearden, Carole A
Sent: Wednesday, August 03, 2016 1:48 PM
To: 'Mutlu Onur' <onur.mutlu@inf.ethz.ch>
Cc: Tewfik, Ahmed H <tewfik@austin.utexas.edu>; Jilda Bolton (jildagayle@gmail.com) <jildagayle@gmail.com>
Subject: RE: Gentle reminder - Promotion Reference letter - Vijay Janapa Reddi
Importance: High

Onur,

The 20th will work but that is the absolute deadline. Our budget council meets early the next and will need that letter before that. We cannot add any letter after they vote.

Cheers,

Carole

From: Mutlu Onur [mailto:onur.mutlu@inf.ethz.ch]
Sent: Tuesday, August 02, 2016 4:43 PM

Onur Mutlu

Full Professor, Systems Group, Department of Computer Science, ETH Zürich, 8092 Zürich, Switzerland
http://www.ece.cmu.edu/~omutlu
omutlu@gmail.com

Research, Teaching and Consulting Interests

- Computer architecture and systems. Memory systems. Multi/many-core systems. Scalable, QoS-aware, latency-tolerant systems.
- Computer architectures for secure and robust operating systems (OS). OS/architecture interaction.
- Architectural support for safe/managed/parallel programming languages (PL) and programmer productivity. PL/architecture interaction.
- Fault tolerant and bug-tolerant architectures. Dependable systems.
- System-wide resource management and QoS, especially in multi-core and multithreaded systems.
- Novel computer architectures for health, biological, medical, and bioinformatics applications.
- Bioinformatics algorithms and architectures. Genome sequence analysis and assembly techniques.

Education

University of Texas at Austin
September 2000 - August 2006
Ph.D., Computer Engineering, August 2006
Dissertation Title: *Efficient Runahead Execution Processors*
Nominated for the ACM Doctoral Dissertation Award by UT-Austin
M.S.E., Computer Engineering, May 2002

University of Michigan, Ann Arbor
September 1997 - August 2000
B.S.E., *summa cum laude*, Computer Engineering, August 2000
B.S., *with highest distinction*, Psychology, August 2000

Professional Work Experience

ETH Zürich, Dept. of Computer Science (D-INFK), Full Professor, ***September 2015 - Present***
Carnegie Mellon University, Dept. of Electrical and Computer Engineering, Adjunct Professor, ***June 2016 - Present***
Carnegie Mellon University, Dept. of ECE, Dr. William D. and Nancy W. Strecker Early Career Endowed (Associate) Professor, ***January 2013 - June 2016***
Carnegie Mellon University, Dept. of Electrical and Computer Engineering, Assistant Professor, ***January 2009 - January 2013***
Carnegie Mellon University, Dept. of Computer Science, Courtesy Professor, ***January 2009 - Present***
Microsoft Research, Computer Architecture Group (Redmond, WA), Researcher, ***August 2006 - January 2009***
University of Texas at Austin, Dept. of Electrical and Computer Engineering, Research Fellow, ***August 2007 - January 2009***
University of Texas at Austin, Dept. of Electrical and Computer Engineering, Research and Teaching Assistant, ***August 2000 - August 2006***
Advanced Micro Devices, Architecture/Performance Modeling Group (Sunnyvale, CA), Co-op Engineer, ***May – August 2005***
Advanced Micro Devices, Architecture/Performance Modeling Group (Sunnyvale, CA), Co-op Engineer, ***May – August 2004***
Intel Corporation, Desktop Platforms Group (Hillsboro, OR), Graduate Technical Intern, ***May – August 2003***
Intel Corporation, Microprocessor Research Labs (Hillsboro, OR), Graduate Technical Intern, ***May – August 2002***
Intel Corporation, Desktop Platforms Group (Hillsboro, OR), Graduate Technical Intern, ***May – August 2001***

Honors and Awards

- Google Faculty Research Award, 2015, 2016
- Microsoft Research Software Engineering Innovation Foundation Award, 2014
- Dr. William D. and Nancy W. Strecker Early Career Professorship, January 2013
- IBM Faculty Partnership Award, 2012, 2013
- Intel Early Career Faculty Honor Program Award, 2012
- Carnegie Mellon University College of Engineering George Tallman Ladd Research Award, 2012
- IEEE Computer Society Technical Committee on Computer Architecture Young Computer Architect Award, 2011
- Hewlett-Packard Laboratories Innovation Research Program Award, 2012
- Nvidia CUDA Center of Excellence Award, 2012, 2013 (with multiple CMU Faculty members)
- Keynote, plenary and invited talks at many conferences and workshops, including ISMM 2016, DAC 2016, NoCArc 2015, CASS 2015, SBAC-PAD 2015, SAMOS 2015, ISC 2015, ASAP 2014, DaMoN 2014, Summer Supercomouting Academy of Moscow State University 2014, IMW 2013, ISMM 2011.
- Best paper award at RTAS 2014
  Bounding Memory Interference Delay in COTS-based Multi-Core Systems
- Best paper award at ICCD 2012 (Computer Systems and Applications Track)
  Row Buffer Locality Aware Caching Policies for Hybrid Memories
- Best paper award at ASPLOS 2010
  Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems

- Best paper award at VTS 2010 (awarded in 2011)
  Concurrent Autonomous Self-Test for Uncore Components in System-on-Chips
- One paper selected as Honorable Mention for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2015
  A Scalable Processing-in-Memory Accelerator for Parallel Graph Processing
- One paper (of 12 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2011
  Kilo-NOC: A Heterogeneous Network-on-Chip Architecture for Scalability and Service Guarantees
- Three papers (of 11 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2010
  Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior
  Aergia: Exploiting Packet Latency Slack in On-Chip Networks
  Data Marshaling for Multi-core Architectures
- Two papers (of 13 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2009
  Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures
  Architecting Phase Change Memory as a Scalable DRAM Alternative
- One paper (of 12 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2008
  Parallelism-Aware Batch Scheduling: Enabling High-Performance and Fair Memory Controllers
- One paper (of 11 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2006
  Diverge-Merge Processor (DMP): Generalized and Energy-Efficient Dynamic Predication
- Two papers (of 13 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2005
  Efficient Runahead Execution: Power-efficient Memory Latency Tolerance
  Wish Branches: Enabling Adaptive and Aggressive Predicated Execution
- One paper (of 15 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2003
  Runahead Execution: An Effective Alternative to Large Instruction Windows
- One paper selected for CACM's "Research Highlights," 2009
  Architecting Phase Change Memory as a Scalable DRAM Alternative
- Best Paper Session (Runner-Up) at HPCA 2015: *Data Retention in MLC NAND Flash Memory: Characterization, Optimization and Recovery*
- Best Paper Session at HPCA 2014: *Improving Cache Performance by Exploiting Read-Write Disparity*
- Best Paper Session at HPCA 2010: *ATLAS: A Scalable and High-Performance Scheduling Algorithm for Multiple Memory Controllers*
- Best Paper Session at HPCA 2009: *Techniques for Bandwidth-Efficient Prefetching of Linked Data Structures in Hybrid Prefetching Systems*
- Best paper award nominations at NOCS 2015, NOCS 2012, HPCA 2015, HPCA 2014, HPCA 2010, HPCA 2009, HPCA 2007, MICRO 2006, and MICRO 2005 conferences
- Selected to the ISCA and MICRO Halls of Fame, 2009
- NSF CAREER Award, 2010 (*QoS-Aware, High-Performance, and Scalable Many-Core Memory Systems*)
- Microsoft Gold Star Award, 2008
- Distinguished Lecture at Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, 28 June 2012.
- PhD Dissertation nominated by UT-Austin for the ACM Doctoral Dissertation Award, 2006
- University Co-op/George H. Mitchell Award for Excellence in Graduate Research (Awarded to 6 out of 271 nominees at UT-Austin), 2005
- Intel Foundation Ph.D. Fellowship, 2004
- University of Texas Graduate School Continuing Fellowship, 2003
- University of Michigan EECS Dept. Summer Research Fellowship, 1999, 2000
- University of Michigan EECS Dept. William Harvey Seeley Award (money award given to the top undergraduate junior), 1999
- University of Michigan Branstrom Freshman Prize, 1998

Publications

(Please visit `http://www.ece.cmu.edu/~omutlu/projects.htm` for electronic copies.)
(Please visit `http://scholar.google.com/citations?user=7XyGUGkAAAAJ&hl=en` for citations.)

Book Chapters

1. Nandita Vijaykumar, Gennady Pekhimenko, Adwait Jog, Abhishek Bhowmick, Rachata Ausavarungnirun, Chita Das, Mahmut Kandemir, Todd C. Mowry, Onur Mutlu,"A Framework for Accelerating Bottlenecks in GPU Execution with Assist Warps," in Advances in GPU Computing and Practice, to be published by Elsevier, 2016.
2. Onur Mutlu, "Main Memory Scaling: Challenges and Solution Directions," in *More Than Moore Technologies for Next Generation Computer Design*, *Springer*, January 2015.
3. Yoongu Kim, Onur Mutlu, "Memory Systems," in *Computing Handbook: Computer Science and Software Engineering*, *CRC Press*, April 2014.
4. Chris Fallin, Greg Nazario, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu, "Bufferless and Minimally-Buffered Deflection Routing," in *Routing Algorithms in Networks-on-Chip*, *Springer*, 2014.
5. M. Aater Suleman, Onur Mutlu, "Accelerating Critical Section Execution with Multi-Core Architectures," in *Multicore Technology: Architecture, Reconfiguration, and Modeling*, *CRC Press*, July 2013.

UNIVERSITY OF ILLINOIS
AT URBANA-CHAMPAIGN

Department of Computer Science
201 North Goodwin Avenue
Urbana, IL 61801-2302 USA

Josep Torrellas
Saburo Muroga Professor
torrellas@cs.uiuc.edu
http://iacoma.cs.uiuc.edu
Phone: 217-244-4148

August 7th, 2016

Prof. Ahmed Tewfik,
Chair, Department of Electrical and Computer Engineering
The University of Texas at Austin

Dear Prof. Tewfik:

This is a letter in response to your request for an evaluation of Professor Vijay Janapa Reddi's scholarly contributions, as he is being considered for tenure and promotion to the position of Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas at Austin. I am quite familiar with Prof. Reddi's professional career, since we both work in overlapping subareas of computer architecture. I know him since he was a graduate student, and have interacted with him often, in conferences, conference program committees, and a variety of professional settings. I have read several of his papers, and seen him present his work at conferences and workshops.

Prof. Reddi's main research area is mobile processor architectures and systems for energy efficiency and performance. After he finished his Ph.D., he was one of the first researchers to spot the important trend toward simpler processor architectures focused on web workloads. He steadily built his research group toward this direction, and he is now one of the leaders in the architecture community in this area. He is well known nationally and internationally, and he is influential in the research community.

Prof. Reddi is well known for his contributions on processor core design (WebCore), on the development of techniques to enhance energy efficiency through reduction in voltage guard-bands and intelligent workload scheduling, on the characterization and measurement of Web-based software systems, and recently, on language extensions for quality of service in this environment. His research is typically characterized by experimental measurements on real processor platforms through oscilloscopes or performance monitors, and then by provide insights and improvements that are both practical and of interest to industry.

As an example, to design processors for web workloads (WebCore), he analyzed real web applications, and then profiled the costly phases in them. Based on the data obtained, he suggested the design of a set of hardware accelerators for some functions, plus simple cores with large instruction caches.

Prof. Reddi's work is influential. It is being followed by other researchers (for example, I do), and by industry. A couple of very good choices he has made in his career so far have been: 1) to

focus mostly on a single research area, and become a leader in it, and 2) emphasize connections with industry. He has spent a lot of effort visiting companies (Intel, AMD, Samsung, ARM, Qualcomm), giving talks there, and working with industry folks. It is always unclear how much of a professor's work directly impacts industry. After all, people in industry try to cover their tracks, to protect themselves from being sued. However, the first sign that you are having an impact is that people in industry are listening, and this is clearly the case for Prof. Reddi. People in companies are certainly listening to his work. I believe that his ideas are having an impact on industry.

Another good strategy of Prof. Reddi is his focus on publishing in the most visible (and competitive) venues. In our field, these are conferences such as ISCA, MICRO, and HPCA. Prof. Reddi has a very respectable number of publications in these venues. This gives him and his department a lot of visibility. It is an outstanding accomplishment indeed. With these works, he also influences the development of our research community.

One of these publications is about the development of a tool for estimating the energy of GPUs. The tool is called GPUWattch. This tool, which Prof. Reddi developed with other researchers, is being widely used in the research community. It has been cited widely. This is another example of Prof. Reddy impact.

Prof. Reddi comes across as expert and ambitious (in a good way). He is very active, organizing workshops or tutorials, participating in panels, and editing visible Special Issues in IEEE magazines. His involvement in the CGO conference, as Program Chair and, in the future, as General Chair is remarkable.

For all these contributions, Prof. Reddi has been justly recognized. First and foremost, he has received the IEEE TCCA Young Computer Architect Award, which is a truly outstanding recognition. He has received research awards from Google and Intel. He has been invited to many top program committees (HPCA, MICRO, ISCA, PPoPP, CGO, and others), which is a clear sign of his high standing in the community. I have had the chance to be in these program committees with Prof. Reddi and find his interventions in the discussion both expert and measured. He has also been invited to speak at several high-ranking university departments. All these are signs of a growing influence in the field.

Prof. Reddi has been able to attract good students and has a good crop of Ph.D. students. He has also been able to get substantial funding for his research. Most notably, a large fraction of his research comes from industry. This is unusual across our field, and is another proof of the relevance of Prof. Reddi's work.

Moving forward, I strongly think that Prof. Reddi will continue to keep his high rate of technical contributions and research funding in the next few years. His research has been evolving from processor centric to more systems oriented. I think that he will take on larger, more systems-oriented projects. He has new research areas that he is looking at, and based on his ambition and past record, I think we will see exciting accomplishments. He will continue to give visibility to your Department.

Overall, I strongly support the promotion of Prof. Reddi to Associate Professor in the Department of Electrical and Computer Engineering at the University of Texas. If he were at my department, I would also strongly support his tenure here. He has an excellent track record of technical accomplishments, and will continue contributing and increasing the visibility of his Department in the years to come.

Sincerely,

Josep Torrellas

Josep Torrellas
Saburo Muroga Professor
Computer Science Department
University of Illinois at Urbana-Champaign

SHORT BIO

Josep Torrellas (http://iacoma.cs.uiuc.edu/josep/cv.html) is the Saburo Muroga Professor of Computer Science at the University of Illinois at Urbana Champaign, where he has been since 1992. He is an IEEE Fellow and an ACM Fellow. He received the 2015 IEEE Computer Society Technical Achievement Award. He has been the Chairman of IEEE Technical Committee on Computer Architecture (TCCA) from 2005 to 2010. Prior to being at Illinois, Torrellas received a PhD from Stanford University.

Torrellas' research interests are computer architectures, technologies and organizations for shared-memory multiprocessors. He has published about 200 refereed publications in top conferences and journals and received over 10 Best Paper Awards. He has graduated 36 PhDs, of which 13 are faculty at leading universities, including Cornell, Washington, Georgia Tech, USC, NCSU, and others. At Illinois, Torrellas is the Director of the Center for Programmable Extreme Scale Computing, and was the Director of the Illinois-Intel Parallelism Center. He is a member of the Computing Research Association (CRA) Board of Directors, and has served as a Council Member of its Computing Community Consortium (CCC).

Jilda Gayle

From: Torrellas, Josep <torrella@illinois.edu>
Sent: Monday, August 8, 2016 12:07 AM
To: Bearden, Carole A; Josep Torrellas
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: RE: Promotion Reference letter - Vijay Janapa Reddi
Attachments: torrellas_reddi.pdf

Dear Prof. Tewfik, Ms. Bearden,

Here is the letter for Prof. Reddi.
I hope it can be helpful, and apologize again for the delay.

Yours sincerely,

Josep

Josep Torrellas
Saburo Muroga Professor of Computer Science
Computer Science Department — torrella@illinois.edu
Univ. of Illinois, Urbana-Champaign — Phone: 217-244-4148
Siebel Center for Computer Science — Fax: 217-265-6582
201 N. Goodwin Ave, Urbana, IL 61801 — http://iacoma.cs.uiuc.edu/~torrellas

---

From: Bearden, Carole A [cjjp@mail.utexas.edu]
Sent: Friday, June 24, 2016 11:39 AM
To: Torrellas, Josep
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Promotion Reference letter - Vijay Janapa Reddi

Dr. Torrellas,

Thank you for agreeing to write a promotion reference letter for Dr. Vijay Janapa Reddi **by August 1, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Janapa Reddi posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

Carole Bearden
Executive Assistant
Electrical and Computer Engineering
The University of Texas at Austin
(512) 471-4540

What starts here changes the world

C

601 N. 34th St
Seattle, WA 98103
+1 617 819 4504
mdw@google.com

Dr. Ahmed Tewfik
Cockrell Family Regents Chair in Engineering
Chairman, Department of Electrical and Computer Engineering
University of Texas at Austin
1616 Guadalupe St.
UTA Building, 7th Floor
Austin, TX 78701

Dear Dr. Tewfik,

It is my pleasure to write this letter in response to your request of an evaluation of Prof. Vijay Reddi for advancement to the rank of associate professor with tenure. Vijay's research is on the boundary between computer architecture and operating systems, and he has built up an exceptional track record in these fields. In particular, his research on optimizing the mobile Web is of high interest to my team at Google, and I wanted to shed some light on the importance of this work to our efforts to improve the Web platform for the next billion mobile users. Vijay is one of the few researchers doing practical, high-impact work on Web optimization, which is a hugely important problem that is the focus of much attention in the industry as well as in academia.

For context, I lead the Chrome Cloud team at Google, which builds cloud-based services to support the Chrome browser. As an example, I responsible for the Chrome Sync service (synchronizing bookmarks, settings, and other data across multiple devices) and the Chrome Data Saver proxy (which compresses mobile Web pages), both of which are in use by hundreds of millions of users. My group consists of about 40 engineers plus product managers, test engineers, and others collaborating on a broad range of projects to make the Web more efficient and useful. Chrome has more than a billion users across both desktop and mobile platforms.

Prior to joining Google, I was a Professor of Computer Science at Harvard, and my research there focused on wireless sensor networks and distributed systems. I joined Harvard in 2003 and was promoted to the position of full professor with tenure in 2010. I received my PhD at UC Berkeley in 2002 and my Bachelors from Cornell in 1996. Vijay was a PhD student advised by Profs. David Brooks and Gu-Yeon Wei during my time at Harvard. Although I did not directly collaborate with him there, I was familiar with his work.

I am primarily familiar with Vijay's research on optimizing the energy efficiency of mobile Web platforms, specifically his work on GreenWeb, WebCore, and browser runtime support. I have sponsored two Google Faculty Research Awards to support Vijay's work in this area. I am not familiar with his other (apparently substantial) research contributions, so I will limit my comments

to his work on the Web platform.

Let me start by explaining the context for the importance of Vijay's work. To say that the mobile Web is important would be an understatement. The last few years have seen vast growth in the use of mobile devices, to the point where mobile usage is now larger than traditional desktop Internet usage. The next billion users who come online, predominantly in emerging markets like Indonesia, India, and China, are going to do so nearly exclusively on mobile devices. For many users, a smartphone will be the only way they ever use the Web.

Of course, the Web was not at all designed with smartphones or mobile networks in mind: it was designed assuming you had a workstation connected to a fast, free network. So, there is this vast and persistent gap between the capabilities of the devices and networks users are using to access the Web, and many of the core assumptions that the Web makes. The Web browser should be thought of as an operating system, and Web pages are really full applications, running (typically) dozens of scripts and rendering code and resources from many different Internet hosts. To make all of this work well, perform well, be energy-efficient, and safe is a tremendous technical challenge.

On Chrome, we care deeply about the energy efficiency of the browser. Mobile users spend a large fraction of their time either browsing the Web directly (within Chrome, or another browser) or interacting with Web content in other apps. For example, most popular apps embed Web pages in some form or another, and many mobile ads are in fact rendered by a small Web browser within the app. So, the energy consumption of the Web platform is of tremendous importance -- Vijay's work is right in the bullseye of the set of problems we care about.

Vijay takes a unique approach to tackling the energy efficiency of the Web by combining novel hardware and software-based techniques. He is one of the few researchers -- indeed, the only researcher to my knowledge -- bringing both architecture and OS ideas to bear on this set of problems. There are vast opportunities for cross-layer optimization on the Web, and Vijay's work is groundbreaking in terms of exploring this space.

For example, Vijay's work on WebCore demonstrates that it's possible to achieve highly efficient rendering of Web content on a dedicated processor, tailored for this purpose. Having this hardware integrated with future mobile systems-on-a-chip would yield higher performance and greater energy efficiency than the standard software implementations today. WebCore applies the concepts of hardware specialization to this domain and we are very interested in exploring how these ideas can be used to inform future SoC and browser designs.

Vijay's work also has a strong bearing on the nascent WebAssembly effort, which is defining a new portable ISA suitable for execution by Web browsers. The idea is that Web application can be compiled to the WebAssembly architecture, and safely executed by Web browsers -- at native speed -- across a wide range of hardware platforms. Incorporating the WebCore principles to this new platform could yield tremendous opportunities for improved energy efficiency and performance.

Vijay's work on GreenWeb complements the WebCore project by providing a software-focused approach that gives Web applications the ability to express quality of service goals and allow the browser runtime to optimize for them. It also explores new techniques for scheduling

operations in a browser to achieve better performance and energy efficiency. I can't overstate how important and difficult this problem is -- we have an entire team at Google focusing on this problem, and the work Vijay is doing is very exciting to us -- we even hosted one of Vijay's PhD students as an intern on the Chrome scheduling team this summer. It is a rare opportunity to really bridge the gap between academic research and real-world application, and applying Vijay's ideas to Chrome has the potential for tremendous impact.

Unfortunately, I am not in a good position to compare Vijay's research output to that of other researchers at a similar career stage, especially since I am not that familiar with the computer architecture community. That said, his publication record is exceptional, with numerous papers in the most selective conferences and journals in his field, and a number of prestigious awards. Vijay has an exceptionally strong track record that spans the architecture, programming language, operating systems, and mobile research communities. His work is creative, impactful, cross-disciplinary, and hugely relevant to important challenges being faced by the mobile industry. I am fully supportive of Vijay's promotion to associate professor with tenure.

Please do not hesitate to reach out if you have any questions or require more information.

Sincerely,

Dr. Matt Welsh
Google, Inc.

http://www.mdw.la/

Jilda Gayle

From: Matt Welsh <mdw@mdw.la>
Sent: Wednesday, July 27, 2016 12:23 AM
To: Bearden, Carole A
Cc: Tewfik, Ahmed H; Jilda Bolton (jildagayle@gmail.com)
Subject: Re: Promotion Reference letter - Vijay Janapa Reddi
Attachments: VijayReddiTenureLetter-July2016.pdf

Dear Carole and Dr. Tewfik,

Please find attached a letter in response to your request for evaluation of Prof. Vijay Reddi for promotion to associate professor. I am sorry that this is a day late. Please let me know if you need anything else.

Best regards,

Matt Welsh
Google, Inc.
http://www.mdw.la/
+1 617-819-4504

On Fri, Jun 24, 2016 at 9:44 AM Bearden, Carole A <cjjp@mail.utexas.edu> wrote:

Dr. Welsh,

Thank you for agreeing to write a promotion reference letter for Dr. Vijay Janapa Reddi **by July 25, 2016**. Attached is a formal letter from Dr. Tewfik with a login and password to review all documents for Dr. Janapa Reddi posted on our secure website.

Please let me know if you have any problems reviewing the documents.

Best regards,

Carole

Carole Bearden

Matt Welsh

mdw@google.com / http://www.mdw.la / +1 617 819 4504
Google, Inc., 601 N. 34th St, Seattle, WA 98105

I am a computer scientist and engineering manager at Google, where I work in the areas of mobile computing, distributed systems, and networking. I lead the Chrome Cloud team, which spans multiple subteams: Chrome Sync (synchronizing bookmarks, settings, tab history across a user's devices); Chrome Data Saver (a proxy service to compress web pages); Google Cloud Messaging support in Chrome; and multiple projects to improve Chrome's performance and functionality in emerging markets.

Prior to joining Google, I was a professor of Computer Science at Harvard University from 2003 until 2010, and a senior researcher at Intel Research, Berkeley from 2002-2003. I did my PhD in Computer Science at UC Berkeley (2002) and my bachelor's in Computer Science at Cornell University (1996).

My research interests span a broad range of topics in the space of mobile computing, operating systems, networks, distributed systems, and programming languages.

- Publications and Talks
- Volatile and Decentralized (my blog)
- My curriculum vitae

Check out this blog post for some background on the Chrome Data Saver proxy, and this paper from NSDI 2015 which describes the service in detail.